TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL:

DUAL TRACE SAMPLING UNIT,

TEKTRONIX TYPE 3S1

This copy is a reprint which includes current pages from Changes 1.

HEADQUARTERS, DEPARTMENT OF THE ARMY

JULY 1972

This manual is an authentication of the manufacturer's commercial literature which, through usage, has been found to cover the data required to operate and maintain this equipment. Since the manual was not prepared in accordance with military specifications, the format has not been structured to consider level of maintenance nor to include a formal section on depot overhaul standards.

Change

No. 2

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, DC, 16 April 1986

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL, INCLUDING REPAIR PARTS AND SPECIAL TOOLS LIST: DUAL TRACE SAMPLING UNIT, TEKTRONIX MODEL 3S1 (NSN 6625-00-900-7572)

Current as of 16 April 1986

TM 9-6625-965-14-1, 6 July 1972, is changed as follows:

1. Remove old pages and insert new pages as indicated below. New or changed material is indicated by a vertical bar in the margin of the page.

Remove pages	Insert pages
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13-1 through 13-10	

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WASHINGTON, D.C., *6 July 1972*

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL, INCLUDING REPAIR PARTS AND SPECIAL TOOLS LIST, DUAL TRACE SAMPLING UNIT, TEKTRONIX TYPE 3S1 (NSN 6625-00-900-7572)

SECTION 0

INTRODUCTION

SCOPE

This manual includes installation and operation instructions and covers organizational, direct support (DS), and general support (GS) maintenance. It describes Dual Trace Sampling Unit, Tektronix Type 3S1.

The basic issue items list appears in Appendix B. Appendix B is current as of 19 April 1972.

INDEXES OF PUBLICATIONS

DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine if there are any new editions, changes, or additional publications pertaining to the equipment.

DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are Modification Work Orders (MWO's) pertaining to the equipment.

FORMS AND RECORDS

Reports of Maintenance and Unsatisfactory Equipment. Use equipment forms and records in accordance with instructions given in TM 38-750.

Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 as prescribed in AR 700-58 (Army), NAVSUP Pub 378 (Navy), AFR 71-4 (Air Force), and MCO P4030.29 (Marine Corps).

Discrepancy in Shipment Report. Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38 (Army), NAVSUP Pub 459 (Navy), AFM 75-34 (Air Force), and MCO P4610.19 (Marine Corps).

Reporting of Errors. The reporting of errors, omissions, and recommendations for improving this manual is encouraged. Reports should be submitted on DA Form 2028, Recommended Changes to Publications, and forward direct to: Commanding General, U. S. Army Missile Command, ATTN: AMSMI-MFM, Redstone Arsenal, AL 35809.

Fig. 1-1. Type 3S1 Dual-Trace Sampling Unit.

SECTION 1
CHARACTERISTICS

General Information

The Type 3S1 Dual-Trace Sampling Unit is a 50Ω input dual-channel vertical plug-in unit designed for operation in any of the Tektronix 560-series Oscilloscopes except the Type 560 or Type 561 (it will operate in the Type 561A). The Type 3S1 operates with either sampling or conventional horizontal plug-in units to take full advantage of its DC to 1000 MHz bandwidth. Sampling horizontal units include the Types 3T2, 3T4 and 3T77A. The Type 3S1 unity dot response permits random sampling displays without overshoot or undershoot for full graticule signal changes in one dot. Conventional horizontal units include the Types 2B67, 3B1, 3B3, 3B4 and 3B5 non-digital time bases, and the Type 3B2 Analog/Digital Time Base Unit. The Type 3S1 provides all the vertical information needed for voltage measurements by either Tektronix digital readout system, the Type 567-Type 6R1A, or the Type 568-Type 230.

The Type 3S1 Dual-Trace Sampling Unit is designed to operate within the Type 561A, RM561A, 564, RM564, 567, RM567, 568 and R568 Oscilloscope main frames. Digital readout is available only when the Type 3S1 is operated in a Type 567, RM567, 568 or R568 Oscilloscope main frame. Operation with either conventional or sampling time base units is a new feature of the Type 3S1, allowing either analog displays, or digital readout for both real-time and equivalent time sampling.

Each of the two channels has its own trigger take-off circuit, signal delay line, deflection factor and positioning controls. Sampled signals are presented to both the Oscilloscope CRT and to front panel connectors for external use with auxiliary equipment such as pen recorders. The two channels operate either individually or in one of three combined modes: Dual Trace, A + B (Algebraic addition), or A VERT/B HORIZ (X-Y).

ELECTRICAL CHARACTERISTICS

Digital Unit Compatibility

The Type 3S1 is compatible for operation with all Type 230 Digital Units and all Type 6R1A Digital Units. It is compatible with all Type 6R1 Digital Units SN 694 and up. Type 6R1 Digital Units SN 101-694 (with exceptions beginning at SN 391) require the installation of Tektronix Modification Kit 040-0342-00 when operated with a Type 3S1. See your Tektronix Field Engineer for details.

The following characteristics apply over an ambient temperature range of 0°C to +50°C. These characteristics apply only after the Type 3S1 VERT GAIN control has been properly adjusted for the oscilloscope and after a sufficient warm-up time. For particular system warm-up requirements, refer to the Main Frame oscilloscope instructions manual. A procedure for mating the Type 3S1 to each oscilloscope can be found in the Operating Instructions section of this manual.

ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirement	Supplemental Information
Transient Response Risetime	≤350 ps, 10% to 90% of step pulse signal.	
Aberration and Tilt	≤ + and - 2% in the first 5 ns after step pulse reaches 100%. ≤ + and - 1% after the first 5 ns.	Applies when pulse generator is a terminated Tektronix Type 281 TDR Pulser.
Deflection Factors mVOLTS/DIV Switch Range	2mV to 200mV in 7 steps in a 1-2-5 sequence	
Accuracy	Within ±3% with INVERT/NORM switch at NORM. Within ±5% with INVERT/NORM switch at INVERT	
mV/div VARIABLE Range	≤0.7:1 reduction in deflection when control is turned CCW from CAL position, and ≥2.5:1 increase in deflection when control is turned CW from CAL position.	
Input resistance	50 Ω, ±1 Ω	Measured at DC.

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Characteristics-Type 3S1

ELECTRICAL CHARACTERISTICS (cont)

Characteristics	Performance Requirement	Supplemental Information
Input Signal		
Dynamic Range	+ and -2 volts from ground.	
Safe input overload	+ and -5 volts from ground.	
Tangential noise	≤2 mV at unity dot response ≤1 mV when smoothed.	When making a visual noise reading from the sampling display, the eye interprets a noise value which is neither the RMS nor the peak to peak value. Most observers agree that the displayed noise value is approximately 3 times the RMS value. Thus it is convenient to define "tangential noise" as exactly 3 times the RMS value. The tangential noise value so defined contains about 90% of the trace dots, representing what most people see in a display containing noise.
Voltage Interchannel crosstalk	≤1% P-P when input signal is a step voltage with ≤80 ps risetime.	Unused channel, in which crosstalk is observed, terminated in 50 Ω.
Co-channel Time Coincidence	≤30 ps.	
Dot Response		
NORMAL	Adjustable (at front panel) to Unity.	Full graticule display change in one dot without overshoot or undershoot.
SMOOTH	≤0.3:1 when NORMAL is adjusted to Unity.	First dot of 100% step display moves ≤0.3 the full amount it would move at Unity dot response.
Trace baseline vertical shift with trigger repetition rate change	≤10 mV for trigger rate change from 30 Hz to 100 kHz.	Timing Unit externally triggered.
Dot slash	Vertical dot drift is ≤0.1 div when timing unit is triggered at 20 Hz.	
FREE RUN Frequency	100 kHz ±5%.	
OFFSET OUT		
Range	At least +10 to -10 Volts.	
Relation to DC OFFSET	DC OFFSET Voltage is 0.1 times OFFSET OUT Voltage within 2%.	
Source Resistance	10 kΩ within 1%	
DC OFFSET Voltage Range	At least +1 to -1 Volt.	
A OUT, B OUT		
Amplitude in Volts (Referred to Input)	Signal Input in Volts times $\left(\frac{200}{\text{mVOLTS/DIV setting}}\right)$ within 2%.	Maximum output voltage ±4V.
Deflection Factor (Referred to CRT)	200 mV/displayed div., within 3% in NORM 200 mV/displayed div., within 5% in INVERT	
Source Resistance	10 kΩ within 0.5%.	
Vertical Signal to Digital Unit Amplitude in Volts (Referred to Input)	Signal Input in Volts times $\left(\frac{1000}{\text{mVOLTS/DIV setting}}\right)$ within 3%.	
Internal Trigger Pickoff Signal Amplitude	≥0.12 X Input signal voltage.	Checked with INTERNAL TRIGGER Switch at OFF, due to variations in timing units.
Vertical Position Indicator Lamps	One indicator lamp will be on and the other off when CRT trace is more than one div away from the graticule centerline.	
DOT RESPONSE Controls Range	≤0.95 to ≥1.05 of unity dot response.	
VERT GAIN Control Range	≤9 to ≥13 Voltage gain.	Voltage gain measured between Channel B amp output (P12, pin 3) and the CRT lower vertical deflection plate (P11, pin 17).

ENVIRONMENTAL CHARACTERISTICS

Storage

Temperature- -40°C to +65°C.

Altitude- To 50,000 feet.

Operating

Operating Temperature- 0°C to +50°C.

Operating Altitude- To 15,000 feet.

MECHANICAL CHARACTERISTICS

Dimensions-	Height	6 1/3 inches
	Width	4 5/16 inches
	Length	14 1/4 inches

Approximate dimensions including knobs and connectors.

Construction- Aluminum alloy chassis with epoxy laminated circuit boards. Front panel is anodized aluminum.

Accessories- An illustrated list of the accessories supplied with the Type 3S1 is at the end of the Mechanical Parts List pullout pages.

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NOTES

SECTION 2
TYPE 3S1 BASIC SAMPLING PRINCIPLES

Introduction

This section of the manual provides the basic information required for operation of the Type 3S1. The equivalent-time sampling process is discussed for the benefit of those unfamiliar with sampling techniques. Operating instructions including first time operation are given in Section 3.

BASIC SAMPLING TECHNIQUES

The current state of the electronics art does not permit the direct cathode-ray tube display of fractional-nanosecond low-level signals. Risetimes in the order of 0.35 ns can be displayed on a CRT if the signal amplitude is high enough. This, however, requires signals of several volts minimum amplitude. Millivolt signals can be amplified to the levels required for CRT deflection. An inherent limitation in linear amplifiers is the compromise necessary between bandpass and gain. A high gain amplifier is a low bandpass amplifier; and conversely, wide-band amplifiers are necessarily low gain amplifiers. For any particular configuration, gain times bandpass is nearly a constant so anything done to increase the gain will proportionately reduce the bandpass. Also, attempts to improve the bandpass will reduce the gain. The gain-bandpass product limitation of linear amplifiers restricts the display of millivolt signals on a CRT to the 50 to 150 MHz region.

The sampling technique permits the quantitative display on a CRT of a facsimile of fractional-nanosecond low-level signals. In the sampling technique, many cycles of an input signal are translated into one cycle of low frequency facsimile. The transition takes place at the input, or sampling bridge. Since only the sampling bridge is subjected to the fast risetimes of the input signals, and all the amplification is done to the relatively low frequency facsimile, the performance of a sampling system is not dependent on the gain-bandpass limitations of conventional amplifiers.

However, the sampling technique introduces some limitations of its own. The sampling technique is restricted to repetitive wave shapes of low amplitude (typically in the order of 1 or 2 volts peak to peak) from low impedance sources. Fortunately, most fractional nanosecond signals exist in low impedance environments and are generally low amplitude. Piping the signal from the circuit under test to the input of the sampling system requires a more sophisticated technique than lower bandpass systems. Notwithstanding its limitations, the sampling technique allows the quantitative display of a general group of fast signals that otherwise would defy observation.

A sampling system looks at the instantaneous amplitude of a signal during a specific small time segment, remembers the amplitude, and displays a single dot on the CRT that corresponds to that amplitude. After the system has recovered and stabilized, it again looks at the instantaneous amplitude of a different cycle of the input signal. Each successive look, or sample, is at a slightly later equivalent time relative to the input signal. Each sample is followed by a spot displayed on the CRT. Generally the vertical position of the spot represents the amplitude of the input signal at sample time, and the horizontal position of the dot represents the equivalent time on the waveform when the sample was taken. After many cycles of the input signal, the sampling system has reconstructed and displayed a single facsimile made up of many samples, each sample having been token from a different cycle of the input signal.

Fig. 2-1 illustrates the reconstruction of a repetitive square wave. The CRT display is a series of dots rather than the conventional continuous presentation. In the illustration, a series of samples is taken from the input signal. The samples, and not the actual input signal, are displayed by the oscilloscope

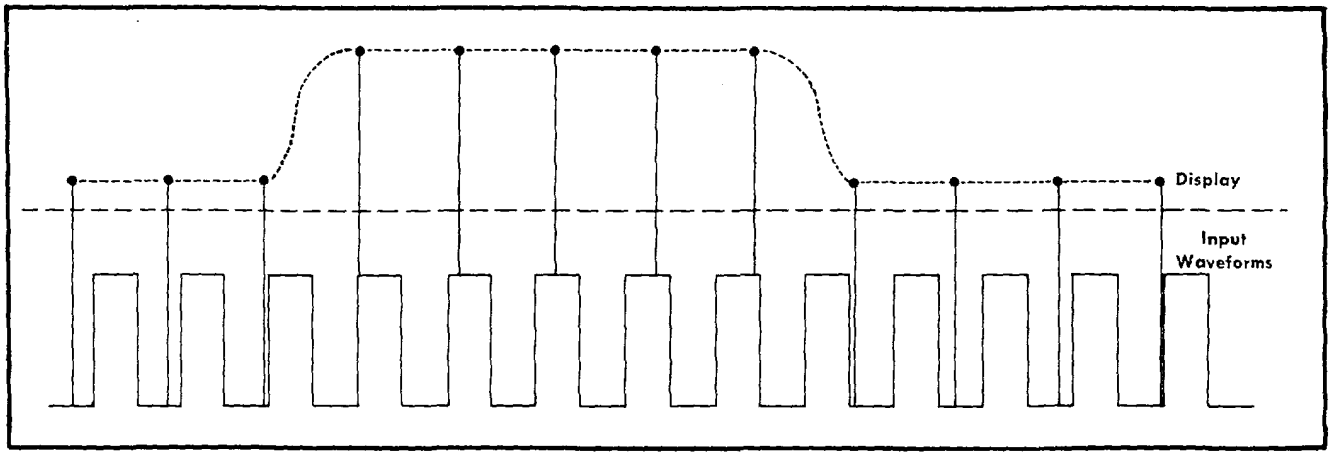

Fig. 2-1. Displaying input waveforms by means of the sampling technique.

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After each sample, when memory has been established and stabilized, the oscilloscope is unblanked and a dot appears. A large number of such dots form the display.

The number of dots per horizontal unit of display is called dot density. The dot density of a display is controlled by the operator to provide the best compromise between resolution and repetition rate of the display. Since only one sample is taken from any particular input cycle, the time required to reconstruct a display is a function of the dot density selected and the repetition rate of the signal. The higher the dot density selected for resolution, the longer the time required to reconstruct a waveform. The higher the repetition rate of the signal, the less time required to reconstruct the waveform up to the maximum repetition rate of the system.

The sampling technique requires repetitive input signals although not necessarily signals with a constant repetition rate. The horizontal position of the spot is determined by the time delay between the point on the signal at which triggering occurred, and the point at which the sample was taken. Since both time references (trigger time and sample time) are taken from the same cycle of the signal, the signal does not have to be periodic. Each cycle of the signal does have to be identical in amplitude, time duration, and shape. Any differences in the individual cycles of the input signal will show in the reconstructed display as noise or jitter.

Sampling systems have a maximum repetition rate at which they can take samples and faithfully display them. The primary limit is the time required for the preamp and the AC amplifier to stabilize after a sample has been taken.

Signals below 100 kHz may have considerable repetition rate jitter and still be presented without display jitter. For signals with a repetition rate higher than 100 kHz, the timing unit holds off retriggering for a minimum of 10 ms. This means that a sample will not be taken from each cycle of a high repetition rate signal. Only those cycles occurring after the holdoff will be sampled. If the signal is truly repetitive and each cycle is identical, these "missed" cycles are of little significance.

The Type 3S1 sampling unit is an error-sampled feedback system with a ratchet memory. The memory output is not reset to zero after displaying a dot. The memory output remains at the displayed amplitude until it is corrected by the next sample. Fig. 2-2 shows a simplified block diagram of an error-sampled feedback system with a ratchet memory. The output from the sampling bridge is the difference or error between the instantaneous amplitude of the signal at sample time and the memory feedback level. A change is made to the memory level only when the instantaneous amplitude of the signal at sample time is different from the memory level. The memory level "ratchets" up or down at each sample time as a result of the error signal sampled. The transition of memory from one level to another occurs between displayed dots and is therefore not seen on the CRT.

The error-sampled ratchet-memory technique has the advantage of allowing smoothing. Smoothing is used to reduce the effects of random noise on the display. It will be discussed later in this section. The error-sampled approach also has the advantage of reducing kickback into the input cable by the interrogate pulse. Since the sample is always the difference between the signal and the memory level, the error signal is much smaller in amplitude than would be the case if memory reverted to zero each time and the entire signal was sampled.

The output from the bridge at sampling time is the difference between the signal level and the memory level. The difference is the input to the amplifier. The output of the amplifier is AC coupled to a memory gate. The memory gate couples the signal to the memory amplifier during the time it is gated on. The memory amplifier changes the memory feedback level in accordance with the error signal.

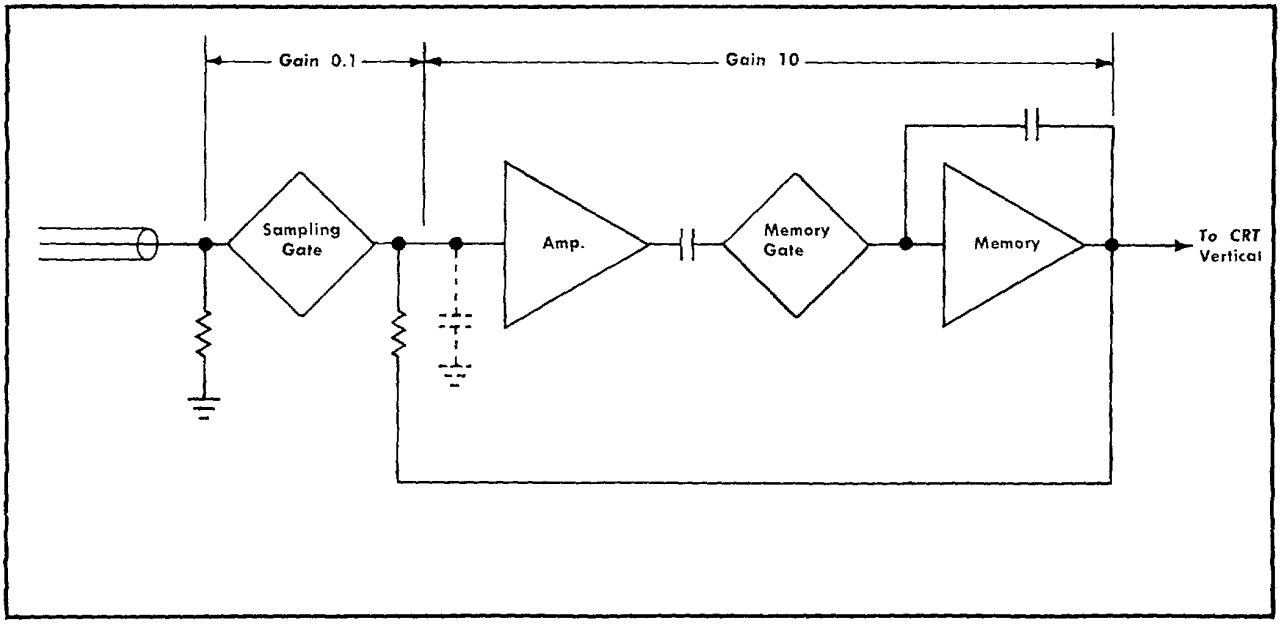

Fig. 2-2. Simplified block diagram of an error-sampled feedback system with a ratchet memory.

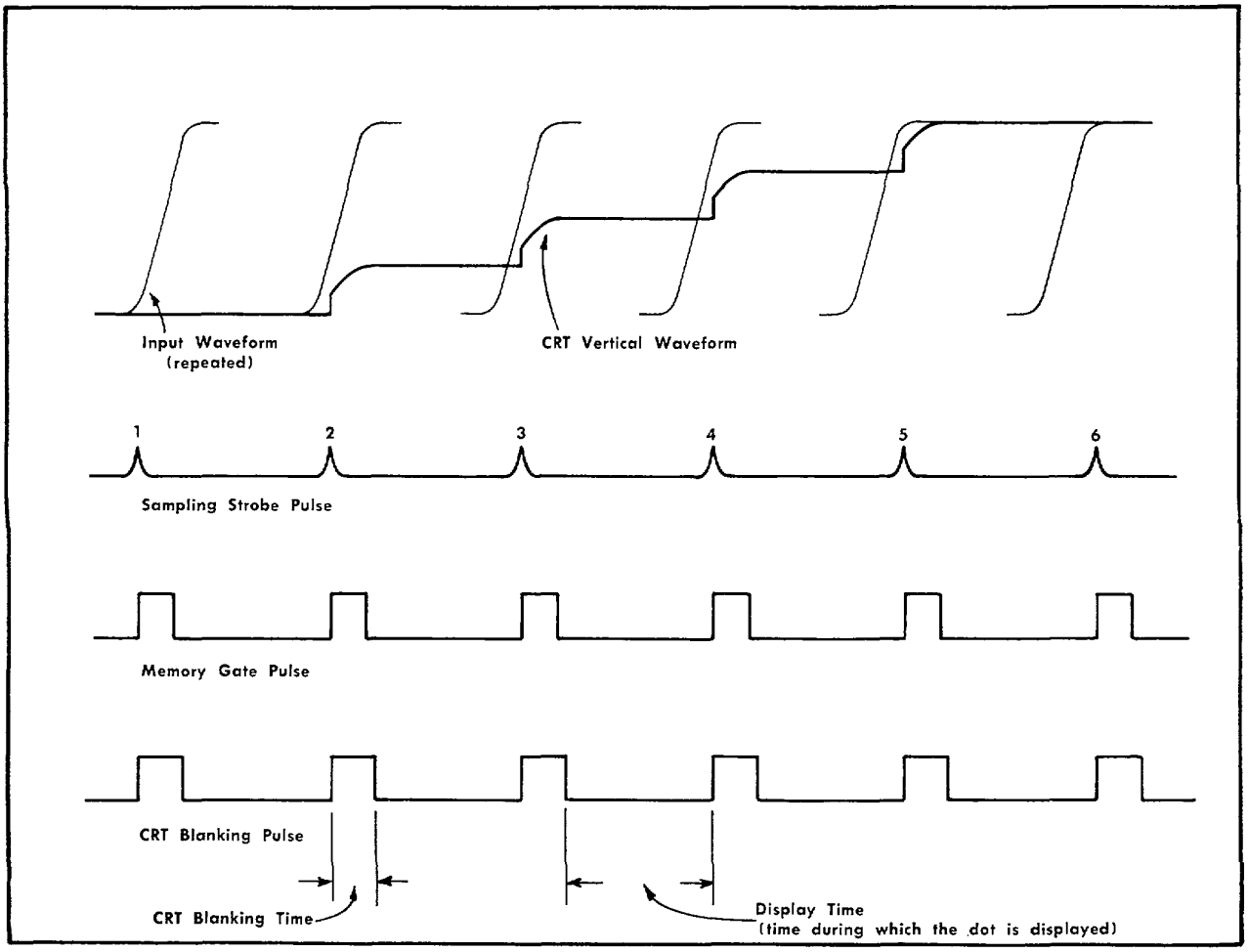

Fig. 2-3. Simplified representation of an error-sampled ratchet-memory waveform.

These changes in memory level occur when the CRT is blanked and therefore do not show up on the display. The memory level does not revert to zero, but remains at the displayed level until corrected by the next error signal. The input to the amplifier of a typical sampling system charges to about 10% of the error signal sampled by the bridge. This percentage of response, or attenuation through the sampling bridge, is known as sampling efficiency. The amplifier and the memory amplifier have a gain of 10. Therefore, the memory feedback level is corrected to equal the signal that was sampled. At each sample time, the difference between the memory feedback level and the signal level is amplified and applied to the memory circuit via memory gate to correct the memory feedback level. This causes the memory level to follow a rising waveform in a series of steps or ratchets as shown in Fig. 2-3. This figure shows the input signal and feedback voltages for 6 samples along the rise of a step waveform.

At the time of sample 1, the input signal and the feedback voltage are equal. There is no error voltage, so the memory level is not changed. The CRT is blanked until the circuit is stabilized.

At the time of sample 2, the input signal is (for example) 0.25 volts. The memory level is 0. Assuming a sampling efficiency of 10%, the input of the amplifier responds to 10% of the difference or 0.025 volts. The 0.025 volts of error signal times the gain of the amplifiers (X10) corrects the memory feedback level to the value of the signal at sample time, 0.25 volts. Again, the CRT is blanked during this change until the circuit is stabilized.

At the time of sample 3, the difference between the input signal and the feedback level is again 0.25 volts. The amplifier input responds to 10% or 0.025 volts. The gain of the amplifier changes the memory level by 0.25 volts to the new value of 0.5 volts (equal to the signal level at sampling time). Again the CRT is blanked during this change, until the circuit is stabilized.

This process continues until sample 6. There is no difference between the input signal at sample 6 time and the feedback level. There is no error signal, and the memory feedback level is not changed. The system will remain at this voltage level until the input level changes, or until system drift has created an error signal.

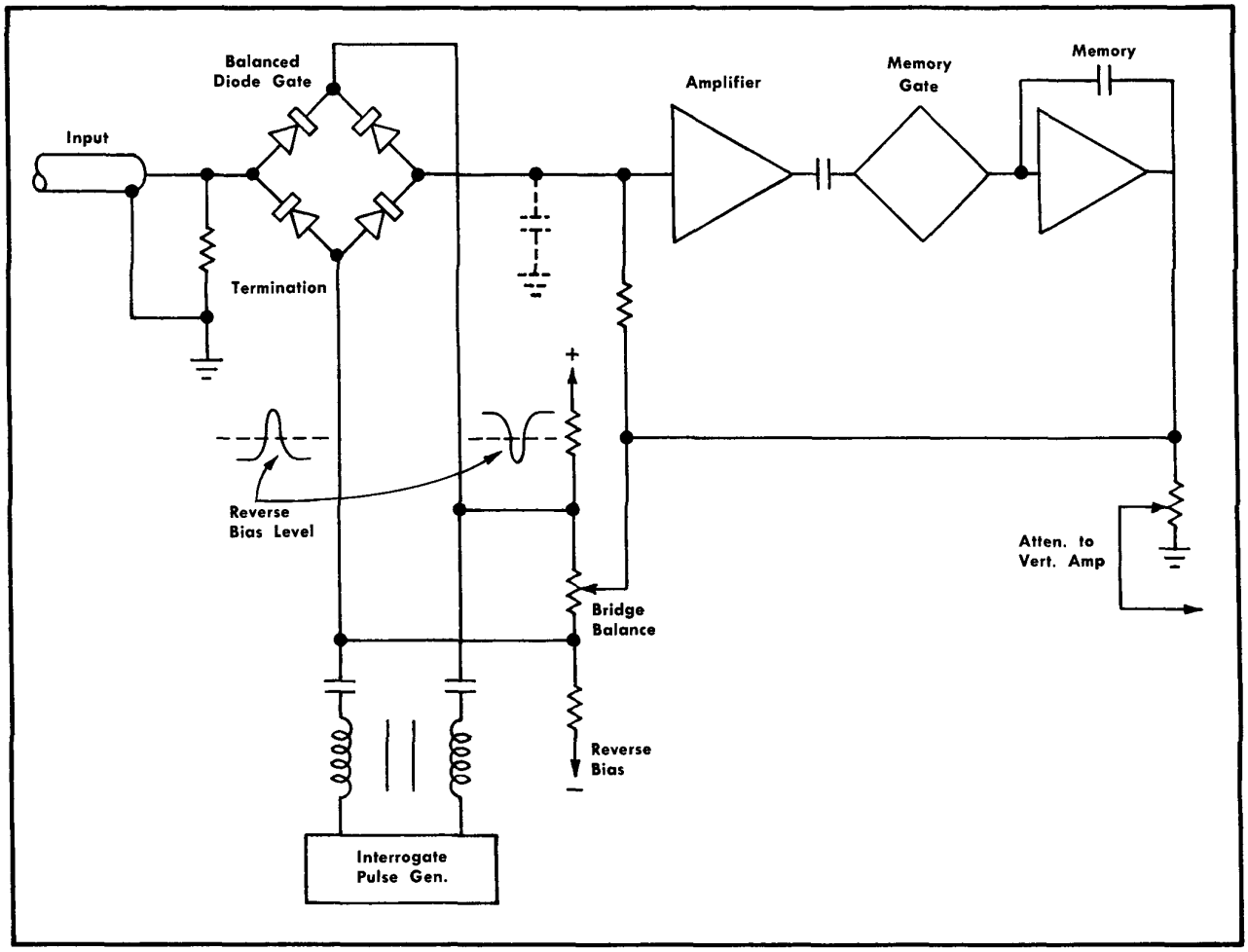

Fig. 2-4. Simplified diagram, showing how the interrogate pulse opens the sampling gate.

Effective Sampling Time

The length of time the input signal is connected to the input of the amplifier by forward bias on the bridge diodes is the practical limiting factor of the minimum risetime a sampling system can display. The duration of the bridge forward bias is controlled by the length of time the interrogate pulse exceeds the fixed reverse bias. Special circuitry is used to make the interrogate pulse as short as possible consistent with noise and diode recovery time. The interrogate pulse is generated by a snap-off diode and a short clip line. The effective duration is adjusted primarily by controlling height and width of the interrogate pulse, thus controlling the time and amplitude by which the interrogate pulse exceeds the reverse bias. Adjusting the reverse bias is a secondary means of controlling the effective duration. Fig. 2-4 shows how the interrogate pulse breaks through the reverse bias on the sampling bridge. The reverse bias is shown by dashed lines through the interrogate pulses.

Dot Response

Dot response refers to the ability of the system to reduce the error voltage to zero after each sample. When the gain of the memory feedback loop is equal to and compensates for the attenuation across the sampling bridge, the dot response is unity or 1. In this case, the memory feedback level will be corrected to equal the level of the signal during the sampling strobe time.

If the dot response is less than unity, the memory level will be corrected by an amount less than that necessary to reduce the error voltage to zero. The memory feedback level will approach the signal level asymptotically. The error voltage will approach 0 after several samples, being reduced by the same factor after each sample. In the case of a dot response of less than unity the memory feedback level is effectively a moving average of several preceding samples.

If the dot response is more than unity, the memory level will overshoot the signal level after each sample. The displayed dot sequence will give the appearance of ringing at the equivalent sampling rate.

For best displayed risetime capability the dot response must be unity allowing the system to track the input signal as closely as possible.

A dot response of less than unity can be useful providing the resulting compromise is understood. The effective averaging

of several consecutive samples caused a dot response of less than unity, serves to reduce the effect of random noise on the display. The averaging also may slow down the fastest display risetime capability, depending upon the number of dots contained in the step transition and the dot response. By increasing the number of dots in the step transition, the display will follow closer to the actual step transition.

Fig. 2-5 shows the displayed waveform with and without smoothing for two different sampling densities Sampling density is the number of samples or dots per division. In the Type 3S1 the operational choice of dot response is either 1.0 (NORMAL) or 0.3 (SMOOTH). In Fig. 2-5A the actual risetime (between the 10% and 90% points) in the NORMAL position takes 5 steps. In the SMOOTH position 7 steps are required. This shows a significant difference in the displayed risetime (SMOOTH) and the actual risetime (NORMAL).

In Fig. 2-5 the sampling density is increased, showing the same number of samples in the SMOOTH and NORMAL positions between the 10% and 90% points of the step transition.

When the smoothed mode has a dot response of 0.3 as in the Type 3S1, 15 or more samples between the 10% and 90% points of a risetime will result in the smoothed and unsmoothed displays having essentially the same risetime. When the smoothed display contains 12 samples between the 10% and 90% points, the smoothed risetime will be about 6% longer than the unsmoothed display. As the number of samples contained in the risetime is reduced below 12, the error between smoothed and unsmoothed display goes up rapidly.

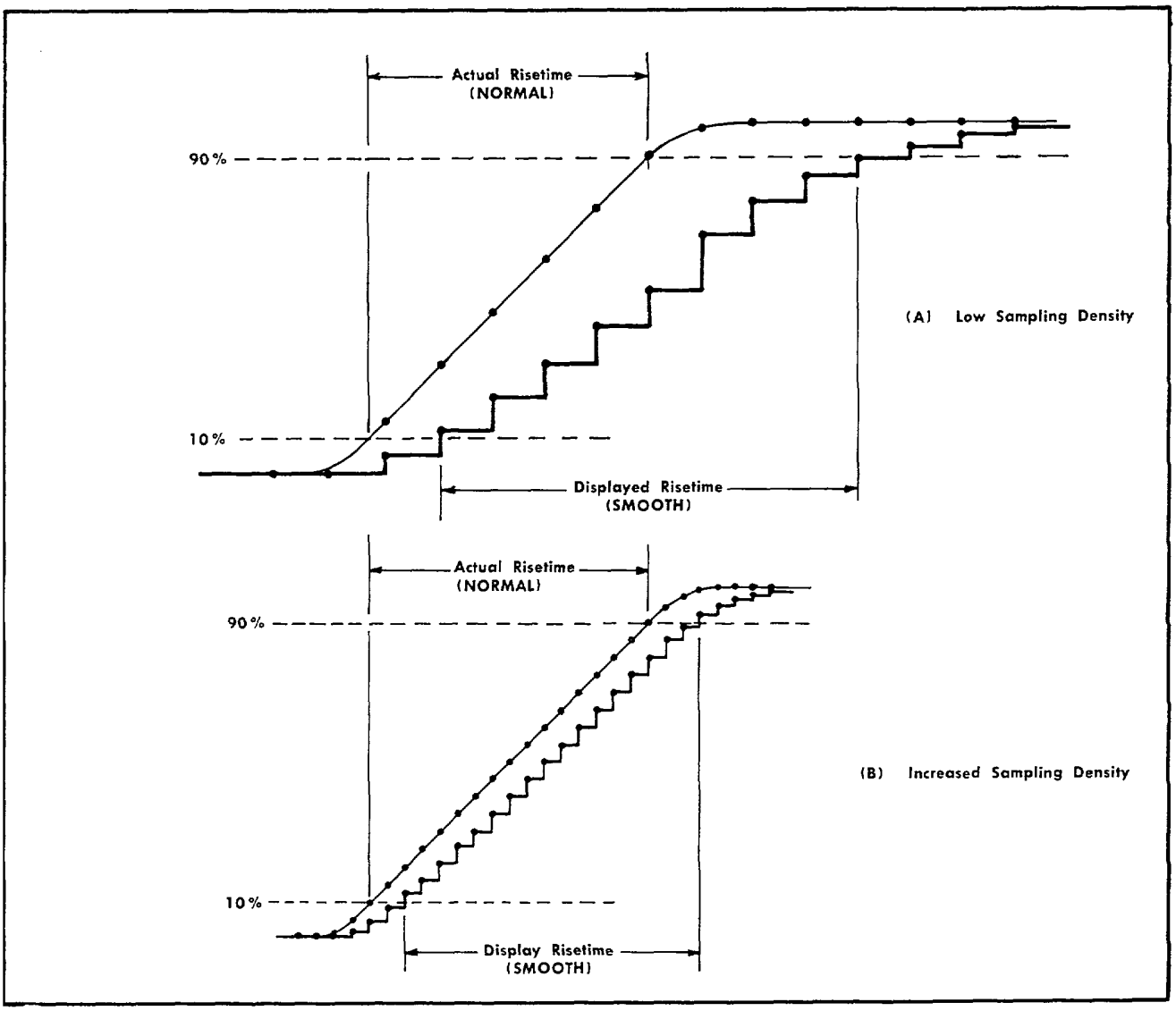

Fig. 2-5. Displayed waveform with and without smoothing for two different sampling densities.

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Smoothing of Random Noise

When the dot response is reduced to 0.3, the displayed dots will represent the average of several consecutive samples. Noise of a random nature will be materially reduced in the display at the possible expense of introducing an error in the displayed risetime. Therefore, if random noise is apparent, reducing dot response may improve the display. Note that this is only true for random noise. Systematic noise (noise with the same repetition rate as the signal) is treated as part of the signal.

The Type 3S1 has a dot response control labeled SMOOTH-NORMAL. In the SMOOTH mode, dot response is reduced to 0.3. Always check that there is sufficient sampling density to warrant smoothing. This can be done by changing the dots/division (or samples/division) control on the timing unit and observing the effect of sampling density on the displayed risetime.

Smoothing cannot be applied where the full amplitude of each sample is required. In a random sampling mode of a time base like the Type 3T2 each sample requires unity dot response. The display dots are not presented in time sequence and therefore cannot be averaged.

Tangential Noise

Traditionally the amplitude of random noise in an amplifier is qualified by stating the equivalent RMS value of the noise referred to the input of the amplifier. In the case of a CRT display, qualifying the noise amplitude by stating its RMS value is somewhat unsatisfactory. The visible effects of random noise on a CRT display is more nearly 3 times the RMS value of the noise. Peak-to-peak value of truly random noise would have to be stated as - infinity to + infinity. Obviously these broad limits would reveal nothing about the amount of noise to expect on a display. It has been determined empirically that 90% of the

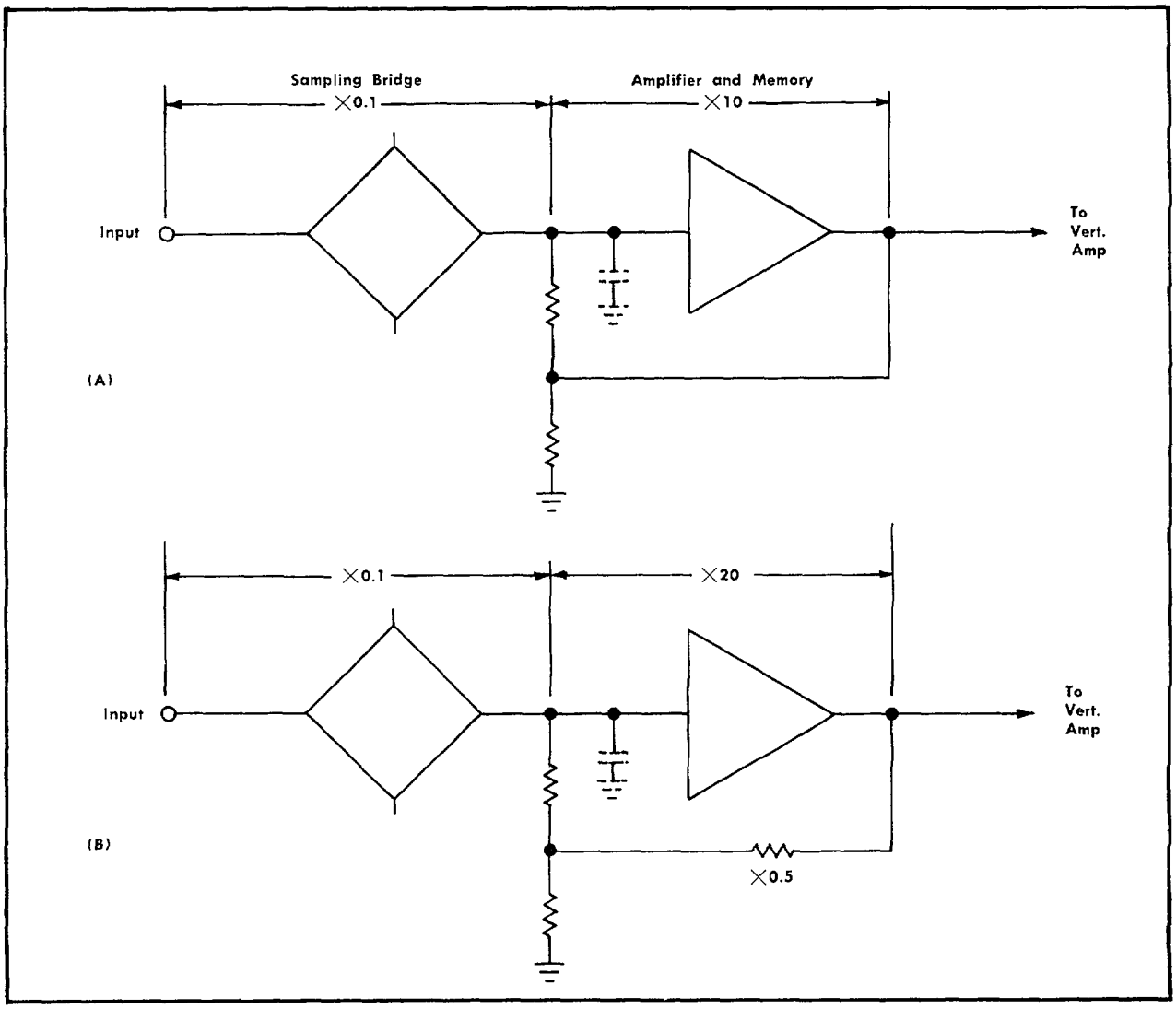

Fig. 2-6. Method of increasing display sensitivity while maintaining unity dot response.

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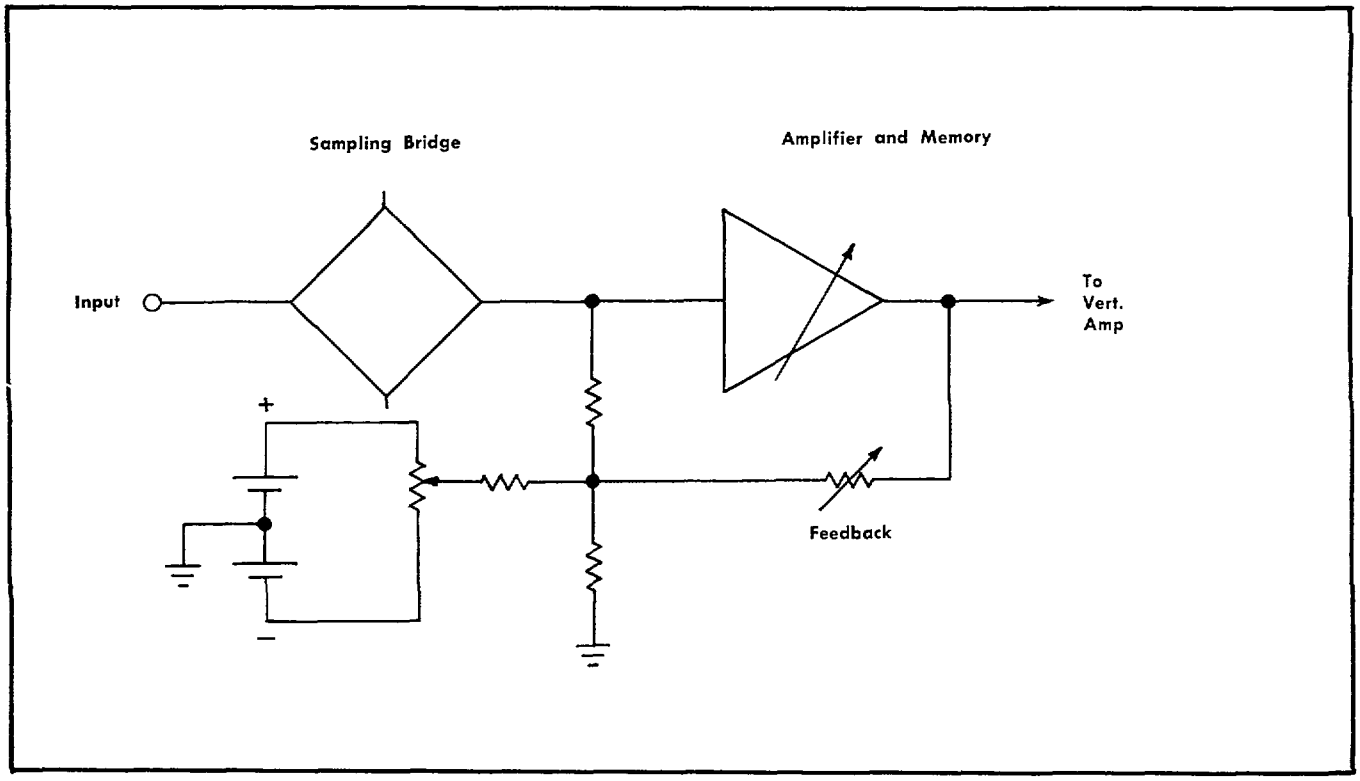

Fig. 2-7. Method of adding a DC voltage to the memory feedback.

dispersion caused by random noise closely approximates the visible widening of the trace. The noise can be described as the separation of two horizontal tangents representing the upper and lower limits of the effective trace width. Hence the term TANGENTIAL NOISE. Tangential noise is defined as an equivalent peak-to-peak voltage at the input of a sampling system that will cause the same trace widening as 90% of the random noise. 5% of the dots would be expected to fall above the trace width and 5% below it. This method of stating the noise figure of a sampling system is considered to be more meaningful than the RMS value, in that it more closely approximates the actual observed trace widening.

Display Sensitivity

Fig. 2-6A shows a simplified block diagram of a bridge and amplifier combination where the gain of the amplifier just compensates for the attenuation at the sampling bridge. In Fig. 2-6B the amplifier has twice as much gain as is necessary to compensate for the low sampling efficiency. By introducing a 2:1 attenuator in the feedback path between the output of the memory amplifier and the output of the bridge, the dot response is still maintained at unity but the output of the memory amplifier is twice as much as the input signal.

Therefore:

(1) The ratio of the feedback attenuator determines the display sensitivity of the system. Given enough samples, the memory feedback to the bridge will always approach the signal level regardless of the forward gain of the amplifier.

(2) The dot response is determined by the combined forward gain of the amplifier and the feedback attenuation ratio. Dot response is controlled by changing the forward gain of the amplifier, independent of the feedback ratio.

(3) To change the display sensitivity without changing the dot response, both the forward gain of the amplifier and the feedback attenuation ratio are changed by the same factor, as shown in Fig. 2-7. This results in a change in the output of the memory amplifier amplitude, but does not change the dot response.

DC Offset

Since the sampling bridge can operate linearly over a range of +2 to -2 volts of input signal, and the system has resolution capability of 2 mV/div, it is advantageous to be able to display a small vertical "window" of the input signal. Fig. 2-7 shows the method of adding a DC voltage to the memory feedback. The error signal that is produced at sampling time is no longer referenced to ground. Instead, it is referenced to the DC offset voltage. The memory feedback voltage produced is therefore the difference between the DC offset and the input signal. The selected deflection sensitivity is then centered around the DC offset voltage instead of ground.

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Real-Time Sampling

Real-time sampling is a method of operation in which the samples are taken at a constant rate from relatively low frequency signal (DC to 20 kHz approximately) and displayed at a sweep rate determined by the Time/div switch on the time-base plug-in. Thus, the samples are taken continuously rather than one sample from each cycle of the signal, and the displayed series of dots follows the actual shape of the input signal waveform.

In real-time sampling operation, the vertical signal provides the trigger to start the sweep. The display, however, is composed of samples at the free-running rate of the dual-trace driver multivibrator.

Sweep Rates

The range of sweep rates available for use in real-time sampling is from the slowest rate provided by the real-time sweep plug-in to about 0.1 ms/div. At this sweep rate, the 100 kHz sampling rate will provide about 100 samples/sweep. At faster sweep rates above 0.1 ms/div, the display dots begin to have significant horizontal dimension due to their duration in real time, and interpretation of the display becomes difficult.

The characteristics of real-time sampling, in addition to slow sweeps at full bandwidth, are reduction of random noise in the display through smoothing, and DC offset capability matched with good overload recovery.

SECTION 3
OPERATING INSTRUCTIONS

General Information

This section covers the operation of the front-panel controls and connectors, installation and first-time operation of the Type 3S1.

The Type 3S1 (with a sampling sweep plug-in unit) converts any Type 561A, RM561A, 567, RM567, 564, RM564, 568 or R568 Oscilloscope into a dual-trace sampling system. The system is self contained, has internal trigger and signal delay, and normally does not require an external trigger. For real time sampling operation, the Type 3S1 can be used with all real time sweep plug-in units such as 2B67, 3B1, 3B2, 3B3, 3B4 and 3B5.

The calibrated deflection factors of 2 to 200 mV/div, together with probes and plug-on external attenuators, adapt to a wide range of input signal levels.

INSTALLING THE TYPE 3S1 IN THE OSCILLOSCOPE

The Type 3S1 is designed to drive the vertical deflection plates of the oscilloscope CRT, and therefore must be used in the left-hand compartment of the oscilloscope.

To insert the Type 3S1 into the compartment, place the latch at the bottom of the front panel in a horizontal position. Then slide the Type 3S1 completely into the compartment. Once the plug-in unit is seated, turn the aluminum knob a few turns clockwise until it is hand-tight.

Mating

If accurate gain measurements are required, the VERT GAIN control can be adjusted with an accurate source voltage to mate the Type 3S1 to the oscilloscope. Refer to Gain Adjustments instructions in this section.

FUNCTION OF FRONT PANEL CONTROLS AND CONNECTORS

Type 3S1 Unit below SN B040740 have the Red HORIZ PLUG-IN control labeled SAMPLING MODE. The two control positions related to the knob, NON-SAMPLING 2B, 3B-SERIES and SAMPLING 3T-SERIES are labeled FREE RUN and TRIGGERED, respectively. Wherever text references are made to the above control, these changes should be noted.

Display Mode Switch	Selects one of five display modes.
CHAN A	The Channel A signal is displayed.
CHAN B	The Channel B signal is displayed.
DUAL TRACE	Alternate samples of Channel A and Channel B are presented.
A + B	The algebraic sum (+A+B as selected with the INVERT-NORM switches) of the two channels is displayed.
A VERT B HORIZ	The Channel A signal is displayed vertically and the Channel B signal is displayed horizontally for X-Y operation.
SMOOTH-NORMAL SWITCH (Red knob concentric with the Display Mode Switch)	Selects unity dot response in NORMAL, and 0.3 dot response in SMOOTH. NORMAL provides the correct displayed risetime for all sampling dot densities. SMOOTH reduces the effect of random noise on the display while requiring high sampling dot density for the correct displayed risetime.
POSITION CONTROLS	Adjusts the vertical position of the A and B displays independently. (The B position control becomes the horizontal position control in the A VERT B HORIZ mode).
POSITION Lights (two indicator lights with indicating arrows in the center of the panel)	Indicate the position of the beam vertically. Helpful in locating the trace when it cannot be seen on the CRT face.
mV/DIV SWITCHES	Select calibrated deflection factor for either channel. For example, with the channel A mV/DIV switch set at 100, each major division of deflection corresponds to 100 millivolts of applied signal at the A INPUT connector when the VARIABLE control is in the CAL position.
VARIABLE CONTROLS	Provides uncalibrated variable adjustment of the deflection factor between the increments of the mV/DIV switches. The variable controls can increase the sensitivity up to a factor of 2.5 or decrease the sensitivity to a factor of 1.4.
DC OFFSET CONTROLS	Control the offset voltage between +1 and -1 volts. These controls are used to offset a known DC component of an applied signal so that a small portion of its amplitude may be displayed at a higher sensitivity than would be possible by use of the vertical position controls. By monitoring the voltage at the appropriate OFFSET OUTPUT jack, very accurate voltage measurements may be made by the slideback technique.
OFFSET OUT	The open-circuit voltage at these jacks is 10 times the internal DC offset voltage. The source impedance is 10 kΩ.
A INPUT and B INPUT connectors	Connectors for applying the input signal to Channel A and Channel B respectively. The input impedance is 50Ω.

Ⓐ 1

Fig. 3-1. Front panel of the Type 3S1.

A OUT .2 V/DIV, 10 kΩ jack	The Channel A display signal is available at this connector. The open-circuit amplitude is 200 mV per division of deflection when the VARIABLE control is in the CAL position. The VARIABLE control changes the deflection factor to the CRT, but does not change the amplitude of the signal at the A OUT jack. Source impedance at this jack is 10 kΩ. Output is not affected by the DISPLAY MODE switch.
B OUT .2 V/DIV, 10 kΩ jack	Same as A OUT except applies to B Channel.
INVERT-NORM switch	In the NORM position, a positive input deflects the CRT beam upward. In the INVERT position the displayed signal is inverted. When the Display Mode switch is set to A-B, algebraic addition of Channels A and B is obtained. The INVERT-NORM switches determine the polarity of each channel before algebraic addition.
INTERNAL TRIGGER Switch	Selects the source of the internal triggering signal (from either Channel A or B). The switch should be set to OFF if the sweep plug-in is externally triggered, to reduce coupling between units.
HORIZ PLUG-IN	In the SAMPLING 3T-SERIES position (use only with sampling time-base plug-ins), the 3S1 sampling cycle is triggered by the sampling sweep plug-in. In the NON-SAMPLING 2B, 3B-SERIES position (use only with conventional or real time time bases), the 3S1 samples continuously at a rate of 100 kHz.

NOTE

The NON-SAMPLING 2B, 3B-SERIES position permits operation with non-sampling time bases. Sampling time bases will not produce a useful display in the NON-SAMPLING 2B, 3B-SERIES mode. Conversely, the SAMPLING 3T-SERIES mode operates only with sampling time bases.

PROBE CONNECTORS	Provides power for active probes, and accessories.
VERT GAIN	Matches the amplifier gain to the oscilloscope CRT deflection factor.
DOT RESPONSE adjustments	Adjusts dot response to unity when SMOOTH-NORMAL switch is in the NORMAL position.

FIRST TIME OPERATION EQUIVALENT TIME SAMPLING

For Equivalent Time Sampling Operation, use a Sampling type plug-in such as Type 3T77A or 3T2 in the right hand compartment of the oscilloscope. If you are not already familiar with the operation of the oscilloscope and sampling time base plug-in, read the First Time Operation portions of the manuals for these instruments before proceeding.

Single Trace

To display a signal, set the Type 3S1 front panel controls as follows:

Display Mode Switch	CHAN A
A and B POSITION	Midrange
A and B mV/DIV	200
A and B VARIABLE	CAL
A and B DC OFFSET	5 turns from either end
A and B INVERT-NORM	NORM
INTERNAL TRIGGER	A
HORIZ PLUG-IN	SAMPLING 3T-SERIES

Apply the signal you wish to observe to the Type 3S1 INPUT A connector. Be sure the applied signal meets the triggering requirements of the sweep plug-in unit, is less than ±1 volt DC, and does not exceed 2 volts peak to peak.

Free run the triggering circuit of the sweep plug-in unit. Center the trace on the graticule with the A POSITION control (and the DC OFFSET control, if necessary). Adjust the triggering controls of the sweep plug-in unit for a stable display and set the channel A mV/DIV switch for the desired amount of vertical deflection.

Now check Channel B by applying the input signal to the B INPUT connector and setting the INTERNAL TRIGGER switch to B and the Display Mode Switch to CHAN B.

Experiment with the various front-panel controls and notice the effect of each. For example, notice that the DC OFFSET control changes the vertical position of the trace, as does the POSITION control. Also the DC OFFSET control varies the voltage at the OFFSET OUT (X10, 10 kΩ) monitor jack. The display may be inverted by placing the INVERT-NORM switch in the INVERT positions.

Dual-Trace

The dual-trace feature of the Type 3S1 permits observing A and B channels simultaneously. This is useful for comparing amplitude, risetime, waveshape, and time relationship of two signals. However, to obtain a stable display of both signals, the signals must be related in repetition rate. When the dual-trace feature is used, be sure to trigger from the channel with the earliest signal event. Use cables with equal delays to preserve the time relationship of the two signals.

Set the controls of the 3S1 for dual-trace operation as follows:

Display Mode Switch	DUAL-TRACE
A and B POSITION	Midrange
A and B mV/DIV	200
A and B VARIABLE	CAL
A and B DC OFFSET	5 turns from either end
A and B INVERT-NORM	NORM
INTERNAL TRIGGER	A or B
HORIZ PLUG-IN	SAMPLING 3T-SERIES

For External triggering, set the INTERNAL TRIGGER switch to OFF. Be sure the external trigger signal is early enough to start the sweep so the vertical signal can be observed.

A + B

For A + B operation set the controls as in Dual Trace operation with these exceptions

Display Mode Switch	A + B
A and B INVERT-NORM	INVERT or NORM

Selection of the INVERT OR NORM position of either A or B Channel will select the polarity of each channel before algebraic addition.

A VERT B HORIZ

For A VERT B HORIZ operation set the controls as in Dual Trace operation with these exceptions.

Display Mode Switch	A VERT B HORIZ
A and B INVERT-NORM	INVERT or NORM

A Position will control the vertical position while B Position will control the horizontal position of the trace. Selection of the INVERT or NORM switch of either channel will select the polarity of the signal on the vertical or horizontal display.

FIRST TIME OPERATION - REAL TIME SAMPLING

For operation of Real Time Sampling use a conventional or real time plug-in time base such as 2B67, 3B1, 332, 3B3, 3B4 or 3B5 in the right hand compartment of the oscilloscope. If you are not already familiar with the operation of the plug-in you are going to use, read the First Time Operation portions of the manuals before proceeding.

Set the controls of the 3S1 for Real Time Sampling operation the same as for the Equivalent Time Sampling Operation in Single Trace, Dual-Trace, and A + B Operation except:

HORIZ PLUG-IN	NON-SAMPLING 2B, 3B-SERIES

INTERNAL TRIGGER may be selected from A or B input by the INTERNAL TRIGGER switch.

Real Time Operation does not permit the A VERT B HORIZ mode. In this position, CHAN A will be displayed vertically.

Incorrect displays can be obtained during Real Time Sampling when the INTERNAL TRIGGER switch is used to internally trigger the Time Base unit. The incorrect displays are possible for either step signals or sine wave signals under the special conditions listed here.

1. The INTERNAL TRIGGER switch is placed to the channel in operation.
2. Step displays of signals with 10% to 90% risetime of approximately 2.5 μs and faster.
3. Sine wave displays of frequencies between 50 kHz and 20 MHz.

Magnitude of display error for step displays will be approximately 6% overshoot at the step transition when the step signal has a risetime of 100 ns or less. The overshoot will decay with a 2.5 μs time constant.

Magnitude of display error for sine wave signals will be approximately 8% too much amplitude (pk-to-pk) at 1 MHz, decreasing to about 2% for both 200 kHz and 10 MHz, and 0% error at about 50 Hz and 20 MHz.

The displays will be correct when the INTERNAL TRIGGER switch is placed to the unused channel (the unused channel can be used for trigger takeoff to the timing unit), or when the switch is placed at OFF and the timing unit is externally triggered. Displays will also be correct for step signals with 10% to 90% risetime longer than approximately 2.5 μs, and for sine wave signals 50 kHz and lower and 20 MHz and higher.

Digital Readout Operation

The Type 3S1 will provide vertical information for use with several different Tektronix Digital Readout systems, such as those including the Type 567 and 6R1A with Type 262 Programmer, or the Type 568-Type 230 system. With either digital system, a time-base plug-in, either sampling or real time is needed along with the Type 3S1. When a real time time-base plug in is used in the system, the A + B and A VERT B HORIZ modes of Type 3S1 operation cannot be used in a digital system. An operational check of digital operation can be found in Steps 18, 19 and 20 in the Performance Check, Section 7.

Gain Adjustment

The VERT GAIN control (a front-panel screwdriver adjustment) matches the gain of the Type 3S1 to the oscilloscope CRT deflection factor. The gain should be checked and adjusted each time the Type 3S1 is used with a different oscilloscope. The setting of the VERT GAIN control should also be checked occasionally during regular use of the instrument.

To check and/or adjust the Type 3S1 VERT GAIN control, proceed as follows:

1. Allow the equipment to warm up for at least 5 minutes.
2. Apply the 0.1 volt signal from the calibrator of the oscilloscope to the A INPUT connector.

NOTE

Early models of 560-series Oscilloscopes may not provide the signal accuracy required for this step without modification.

For a Type 561A Oscilloscope, R898 in the calibrator circuit must be a 100 Ω, 1/2 watt, 1% resistor. If it is not, replace it with one having this value. The 0.5 volt calibrator position will then supply 0.1 volts into 50 ohms.

For a Type RM561A oscilloscope, R898 in the calibrator circuit must be a 250 Ω, 1/2 watt, 1% resistor. If it is not, replace it with one having this value. The 1 volt calibrator position will then supply 0.1 volts into 50 ohms.

For a Type 567 or RM567 oscilloscope, a resistor R890 should be located between the 0.5 volt calibrator jack and the junction of R887 and R888.

The resistor has a value of 100 ohms, 1/2 watt, 1%. If your oscilloscope does not have this resistor, install one at the point indicated (in series with the 0.5 volt calibrator jack). This jack will then provide 0.1 volts into 50 ohms.

3. Free-run the sweep plug-in-unit.

4. On the Type 3S1, set the DISPLAY MODE switch to A ONLY, the A VARIABLE control to CAL, and the A mV/DIV switch to 20. Other controls may be set to any position.

5. With the channel A POSITION and DC OFFSET controls, align the display with the graticule lines and check for exactly 5 major divisions of vertical deflection. If the amount of vertical deflection is not exactly 5 major divisions, adjust the VERT GAIN control.

6. Connect the calibrator signal to the B INPUT connector. Set the Display Mode switch to B ONLY, the Channel B VARIABLE control to CAL, and the B mV/DIV switch to 20. Other controls may be set to any position.

7. With the Channel B POSITION control and the DC OFFSET controls, align the display with the graticule lines and check for 5 major divisions of vertical deflection. If the amount of vertical deflection is not 5 major divisions, refer to the calibration section of this manual.

A OUT and B OUT jacks

The Channel A and Channel B display signals are available at the respective A OUT and B OUT jacks. The signals at these jacks are taken after the sampling process, and are therefore proportional representations of the display signal rather than the input signals themselves. The open circuit voltage at either jack is 200 mV per division of display with the VARIABLE controls in the CAL position. The source impedance is 10 kΩ. The signals are taken prior to the Display Mode switch, and are therefore not affected by the display selected by the Display Mode switch. They ore only affected by the respective mV/DIV switches, DC OFFSET controls, and the SMOOTH-NORM switch. The signals are not inverted by the INVERT-NORM switches, and are not affected by the POSITION controls.

Since the actual waveform duration of the signals at the A OUT and B OUT jacks is much longer than the applied signal, the A OUT and B OUT waveforms are useful for pen recorder applications.

SMOOTH-NORMAL Switch Operation

NORMAL is used to obtain correct displayed risetime for all sampling densities. Displayed random noise can be reduced by setting the SMOOTH-NORMAL switch in the SMOOTH position at the expense of increased risetime at low sampling densities. See the discussion on dot response in Section 2.

Positioning the Display

When making accurate time or amplitude measurements, it is usually advantageous to align the display with the graticule markings. Vertical positioning of the display can be controlled with the appropriate POSITION or DC OFF-SET control.

The effect of the DC OFFSET control is most significant at low deflection factors. As the mV/DIV switch is set to a lower number, the display may be deflected entirely off the CRT. In this case, use the DC OFFSET control to return the display on the CRT. The POSITION control may be used for more precise positioning.

Precise pulse-height measurements can be made by measuring the voltage change at the OFFSET OUT monitor jack as the setting of the DC OFFSET control is changed from one point on the pulse (such at the baseline) to another (such as peak height).

Cable Considerations

If transmission lines or terminations are improper, reflections, standing waves, or undue loading on the device under test may cause signal distortion. If it is necessary to use other than the 50-ohm cables supplied, use suitable matching devices to couple between cables or inputs. Be sure to use only low-loss transmission lines and keep all connections as short as practical to minimize cable losses.

Time delay of cables varies with length and construction. Time delay is especially important when making time difference measurements between two signals, as in dual-trace or X-Y operation. In this case, each signal should travel through cables that produce equal delay to preserve the true time relationship.

Coupling a Signal Into the 50-Ohm Input

To observe the output signal of an instrument having a 50-ohm output impedance, connect a 50-ohm coaxial cable directly between the output of the instrument and either the A INPUT or B INPUT connector. GR Type 874 adapters are available that will mate with most common connectors. If the output of the instrument is other than 50 ohms, use a suitable matching device.

Probes. Special passive or active probes are available from Tektronix for use with the Type 3S1, such as P6034, P6035, and P6045. The P6040 with Type CT 1 and CT 2. Current transformers is available for current measurements.

For further information regarding coupling probes and accessories refer to the Applications Section 4.

NOTES

SECTION 4
APPLICATIONS

Voltage Measurements

Vertical displacement of the trace on the CRT is directly proportional to the voltage at the INPUT connector of the Type 3S1. The amount of displacement for a given voltage can be selected with the mVOLTS/DIV switch. To provide sufficient deflection for best resolution, set the mVOLTS/DIV switch so the display spans a large portion of the graticule. Also, when measuring between points on a display, be sure to measure consistently from either the bottom, middle, or top of the trace. This prevents the width of the trace from affecting the measurements.

To make a voltage-difference measurement between two points on a display, proceed as follows:

1. Note the vertical deflection, in major graticule divisions, between the two points on the display. Make sure the VARIABLE control is in the CAL position.

2. Multiply the major divisions of vertical deflection by the setting of the mVOLTS/DIV switch and the attenuation factor (if any) of external attenuators or probes. The product is the voltage difference between the two points measured.

For example, suppose you measure 4.4 divisions of deflection between two points on the display and the mVOLTS/DIV switch is set at 20. Multiplying 20 millivolts/division by 4.4 divisions, the product is 88 millivolts. This is the voltage at the INPUT connector. Now assume there is a 10X external attenuator (probe) between the INPUT connector and the signal source. To determine the actual signal voltage at the source, multiply 10 (the attenuation factor of the probe) by 88 millivolts; this product (880 millivolts or 0.88 volts) is the actual voltage at the signal source.

If desired, you can measure the instantaneous (or DC) voltage to ground from the display. This measurement is accomplished in the same manner except that, with no signal applied, you must first establish a ground-reference point on the CRT. To do this, allow the sweep plug-in unit to free run and present a trace. Then, position the trace so it is exactly aligned with one of the horizontal graticule lines. The actual graticule line you select will be largely determined by the polarity and amplitude of the applied signal. After establishing the ground reference, make no further adjustments with the POSITION controls.

Apply the signal and measure the voltage in the manner previously described. Make all measurements from the established ground reference point.

If the applied signal has a relatively high DC level, the ground-reference point and the actual signal may be so far apart that neither will appear on the CRT. In this case, refer to the following discussion on "Voltage Measurements Using the DC Offset Control."

Voltage Measurements Using the DC Offset Control

The DC offset voltage cancels the effects of an applied DC level (up to ±1 volt) on the display. Also, accurate slideback amplitude measurements of the applied signal can be obtained by positioning the display at various points and measuring the amount of voltage change at the appropriate OFFSET OUT jack (left hand jack monitors Channel A, right hand jack monitors Channel B).

Source impedance for the voltage at the OFFSET OUT jacks is 10 kΩ; therefore, meter loading may be a factor if a low impedance meter is used. The accuracy of the DC offset voltage measurement depends on the accuracy and the loading effect of the measuring device. The following measuring devices are recommended in the order of preference, for monitoring the voltage at the OFFSET OUT jacks.

(1) Differential, non-loading DC voltmeter with an accuracy of 0.2% or better. This type of device provides 2% accuracy of absolute offset voltage measurements. Measurements of changes in offset voltages can be made more accurately than 2%.

(2) Vacuum-tube voltmeter with an input impedance of at least 10 megohms. Accuracy of the VTVM should be as high as practical.

(3) Zero-center ±1 mA milliammeter with as high an accuracy as practical. The milliammeter should be connected directly between the appropriate OFFSET OUT monitor jack and ground. When using a milliammeter, 100 microamperes is equivalent to 1 volt open-circuit at the OFFSET OUT monitor jack (0.1 volt of actual offset to the signal).

To measure the voltage difference between two points on a waveform (such as peak or peak-to-peak volts), proceed as follows:

1. Set the appropriate DC OFFSET control to about midrange.

2. Apply the signal to be measured to the appropriate INPUT connector. Adjust for a stable display with about 7 divisions of vertical deflection between the two points of the signal to be measured. Make sure the VARIABLE control is in the CAL position.

3. With the POSITION and DC OFFSET controls, move one of the points to be measured to the center line of the graticule and measure the voltage at the appropriate OFFSET OUT monitor jack. Use one of the measuring devices mentioned previously. DO NOT MOVE THE POSITION CONTROL AFTER THIS STEP.

4. With the DC OFFSET control, move the display so the other point to be measured is aligned with the centerline of the graticule and again measure the voltage at the appropriate OFFSET OUT monitor jack.

5. Find the difference between the voltage measured in step 3 and the voltage measured in step 4 and divide by 10. The result is the voltage difference, in volts, between the two points on the waveform.

Applications - Type 3S1

X-Y Phase Measurement

X-Y operation is obtained by placing the DISPLAY MODE switch in the A VERT B HORIZ position. This allows Channel A to control vertical deflection and Channel B to control horizontal deflection.

To produce a Lissajous display of two signals of the same frequency, proceed as follows:

1. Set the Type 3S1 front-panel controls as follows:

Display Mode switch	A ONLY
INVERT-NORM switches	NORM
DC OFFSET controls	midrange
INTERNAL TRIGGER	A or B, as desired

2. Apply one signal to the A INPUT connector and the other signal to the B INPUT connector through equal lengths of coaxial cable.

3. Set the triggering controls of the sampling sweep plug-in unit for a stable display of at least one complete event.

4. Adjust the following Channel A controls, as required, to obtain a centered, 6-division display, mVOLTS/DIV, VARIABLE, DC OFFSET and POSITION.

5. Set the Display Mode switch to B ONLY and repeat steps 3 and 4 using the Channel B controls.

6. Set the Display Mode switch to A VERT B HORIZ.

7. Using both Type 3S1 POSITION controls, position the display on the graticule (both vertically and horizontally) for the type of X-Y display desired.

8. If the input signals are sine waves which produce an ellipse, Fig. 4-1 shows a method of calculating the phase difference between the two signals. If the display appears as a diagonal straight line, the two sine waves are either in phase or 180^{o} out of phase. If the display is a circle, the two sine waves are 90° out of phase.

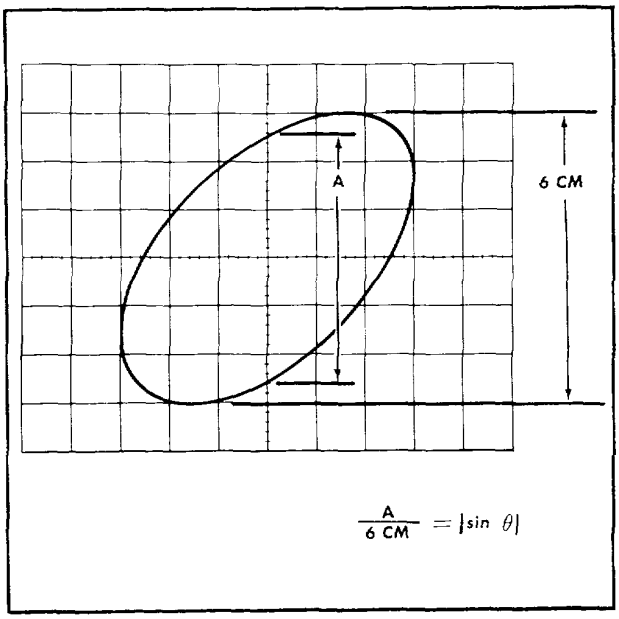

Fig. 4-1. X-Y method of calculating phase difference (0) of two sine waves.

Time Domain Reflectometry (TDR)

When used with a TDR pulser such as the Tektronix Type 281, the Type 3S1 sampling plug-in unit can be useful in pulse analysis of transmission lines.

Algebraic Addition or Subtraction

The algebraic sum of the Channel A and the Channel B signals is displayed when the DISPLAY MODE switch is in the A + B position. Arithmetic addition is obtained when the two INVERT-NORM switches are in the same positions. Arithmetic subtraction is obtained when the two INVERT-NORM switches are in opposite positions. Both the A and B POSITION controls and the A and B DC OFFSET controls affect the display.

The A + B mode of operation is particularly useful for observing waveforms that are not referenced to ground. For example; the current signal across a metering resistor, or the voltage drop across a diode, etc.

The combined Channel A and Channel B signal is not sent to an associated digital unit; rather the two channels are sent to the digital unit independently, even though the Type 3S1 display is the two channels combined.

Dual-Trace Applications

The dual-trace mode of operation allows the simultaneous viewing of two time-related signals on the same time base. The dual-trace presentation makes it possible to make very accurate comparisons of time relationships between two signals. Applications include measuring delay time of delay lines and cables; storage time of transistors and diodes; input to output delay in counters, etc.

Pen Recorder Operation

The signals available at the A OUT and B OUT jacks provide a convenient source for driving the Y axis of a pen recorder. It is common practice to manually scan the CRT (with the sampling sweep plug-in controls) while driving the time axis of the recorder with the sweep output voltage. Another method for pen recording is to couple the scanning voltage of the recorder to the external sweep input connector of the sweep unit. Be sure the sweep voltage from the recorder agrees with the limits of the input to the sampling sweep plug-in.

The source impedance of the A OUT and B OUT jacks is 10 kΩ. This impedance may have to be considered in the calibration of some types of pen recorder amplifiers.

Input Connections

The input circuits for both the A and B channel inputs are 50 ohm transmission lines. 50 ohm coaxial cables may be used for applying input signals with minimum signal loss or distortion.

When connecting a signal to the Type 3S1, many factors must be taken into consideration including loading of the source, losses in the coaxial cables, time delay, AC or DC coupling, attenuation of large signals and matching impedances at high frequencies. This portion of the manual discusses these factors with respect to the vertical input signal.

Coaxial Cables

Signal cables that connect the vertical signal from the source to the Type 3S1 INPUT connectors should have a characteristic impedance of 50 ohms. Impedance other than 50 ohms will cause reflections that may make it difficult to interpret the display. High-quality low-loss coaxial cables should be used to ensure that all the information obtained at the source will be delivered to the Type 3S1 input. If it is necessary to use cables with characteristics impedance other than 50 ohms, suitable impedance-matching devices will aid in the transition.

The characteristic impedance, velocity of propagation and nature of signal losses in a coaxial cable are determined by the physical and electrical characteristics of the cable. Common coaxial cables, such as RG-213/U, have losses caused by energy dissipation in the dielectric proportional to the signal frequency. Some small diameter cables (1/8 inch) lose much of the high-frequency information of a fast-rise pulse in a very few feet of interconnecting cable.

It takes only 6 feet (9 ns delay) of RG-58A/U cable to cause a 10% degradation in risetime. However, it will take about 15 feet (22.5 ns delay) of RG-213/U or 80 feet (95 ns delay) of 7/8 inch Spir-o-line to cause the same amount of change. High quality, low loss signal delays of 60 ns can be obtained by use of a Tektronix Type 113 Delay Cable.

It is important to note that the rise times of step function output signals in coaxial cables deteriorate approximately as the square of the length of the cables. A 1 foot length of RG-58/U has a risetime capability of about 8 ns; a 10 foot length has a risetime capability of about 800 ns. As the length of cable is increased by a factor of 10, the risetime capability deteriorates by a factor of approximately 100.

A coaxial cable does not respond to a fast risetime step function in exactly the same manner as an amplifier with a gaussian roll-off. Therefore, the 10% to 90%, method of stating amplifier risetime capability does not apply when stating coaxial cable risetime capability. Fig. 4-2 illustrates an ideal voltage step function, the output voltage waveform expected from an amplifier with gaussian roll-off, and the output voltage waveform expected from a length of coaxial cable. The output voltage waveform from the amplifier is essentially linear between the 10% and 90% amplitude points, with "knees" at both the beginning and end of the risetime. In the case of the voltage waveform from the length of coaxial cable, the slope of the waveform constantly changes throughout the total risetime. This results in a rapid transition from zero to about the 50% point, and materially longer transition time from the 50% to 100% points.

Input Signal Attenuation

The maximum amplitude that should be applied to the A or B INPUT connectors of the Type 3S1 is ±2 volts, combined DC and peak AC. (Maximum safe input overload is ±5 volts.) If the signal amplitude (into 50 Ω) exceeds ±2 volts, use an attenuator

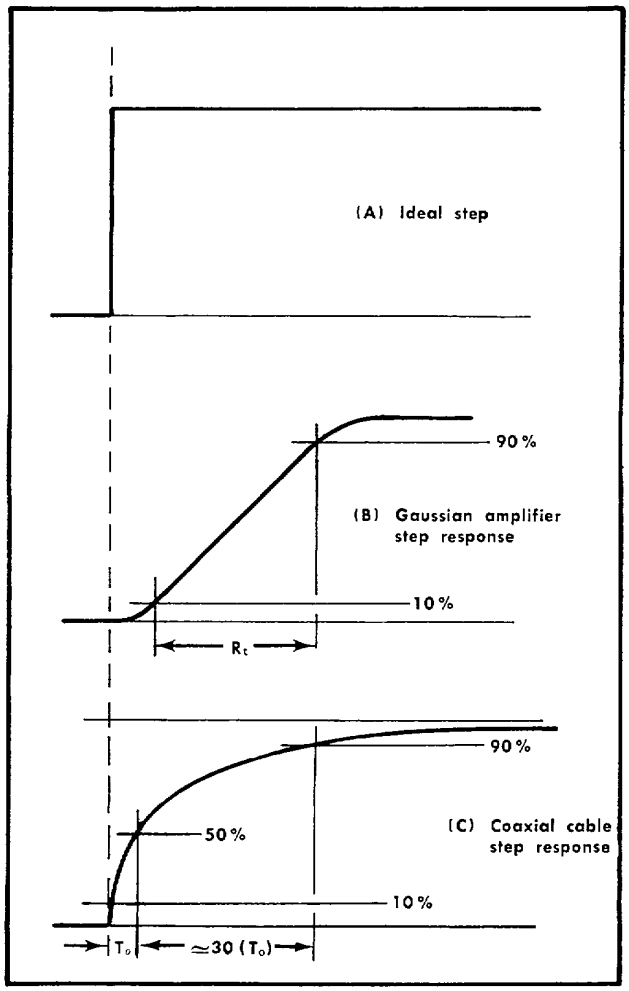

Fig. 4-2. Typical amplifier and coaxial cable response to an ideal step function signal.

probe and/or external coaxial attenuators. The attenuators used must have a flat response to about 2 GHz to avoid reducing the system performance. High-quality 50 ohm coaxial attenuators are available through your Tektronix Field Office or Representative with attenuation factors of 10X, 5X and 2X. When the attenuators are stacked, their attenuation factors multiply; i.e., two 10X attenuators produce 100X attenuation.

Impedance Matching

To provide a smooth transition between devices of different characteristics impedance, each device must encounter a total impedance equal to its own characteristics impedance. Thus, when a signal is applied to the Type 3S1 A or B INPUT connector, if the source impedance of the signal is not 50 ohms, a suitable impedance-matching device must be provided. If the impedances are not matched, reflections and standing waves in the cables will result in distortion of the displayed waveform.

In many cases, insertion of a 50-ohm attenuator in the signal path will provide an approximate impedance match

and will absorb most reflections. It should be noted, however, that the attenuation factor will not be the same as it would be if the impedances were the same on both sides.

Fig. 4-3 illustrates a simple resistive impedance-matching network that provides minimum attenuation. To match impedances with the network, the following conditions must exist:

$\frac{(R_1 + Z_2) R_2}{R_1 + Z_2) + R_2}$ must equal Z_1; and $R_1 + \frac{Z_1 R_2}{Z_1 + R_2}$ must equal Z_2.

Therefore:

$R_1R_2 = Z_1Z_2$; and $R_1Z_1 = R_2 (Z_2 - Z_1)$

$$\text{or } R_1 = \sqrt{Z_2 (Z_2 - Z_1)};$$

$$\text{and } R_2 = Z_1 \sqrt{\frac{Z_2}{Z_2 - Z_1}}$$

As an example, to match a 50-ohm system to a 125-ohm system:

$Z_1 = 50$ ohms; and $Z_2 = 125$ ohms.

Therefore:

$R1 = \sqrt{125 (125 - 50)} = 96.8$ ohms

$$\text{and } R_2 = 50 \sqrt{\frac{125}{125 - 50}} = 64.6 \text{ ohms}$$

Though the network in Fig. 4-3 provides minimum attenuation for a purely resistive impedance-matching device, the attenuation as seen from one end does not equal that seen from the other end. A signal applied from the lower impedance source (Z_1) encounters a voltage attenuation (A_1) that may be determined as follows:

$$\text{Since: } I_{R1} = I_{Z2}; \quad \frac{E_1 - E_2}{R_1} = \frac{E_2}{Z^2}$$

$$\text{Therefore: } A_1 = \frac{E_1}{E_2} = \frac{R_1}{Z_2} + 1; \; (1 < A_1 < 2)$$

A signal applied from the higher impedance source (Z_2) will encounter a greater voltage attenuation (A_2) that may be determined similarly:

$$\text{Since: } I_{R1} = I_{R2} + I_{Z1}; \quad \frac{E_2 - E_1}{R_1} = \frac{E_1}{R_2} + \frac{E_1}{Z_1}$$

$$\text{Therefore: } A_2 = \frac{E_2}{E_1} = \frac{R_1}{R_2} + \frac{R_1}{Z_1} + 1; \; (1 < A_2) < \frac{2Z_2}{Z_1}$$

In the example of matching 50 ohms to 125 ohms,

$$A_1 = \frac{96.8}{125} + 1 = 1.77;$$

$$\text{and } A_2 = \frac{96.8}{64.6} + \frac{96.8}{50} + 1 = 4.44$$

Note that if the 50-ohm source were used for pulsing a high-impedance load, R_1 would approximately equal the impedance of the load (high R) and R_2 would approximately equal the 50 ohms of the pulse source. In this situation, voltage attenuation would be about 2.

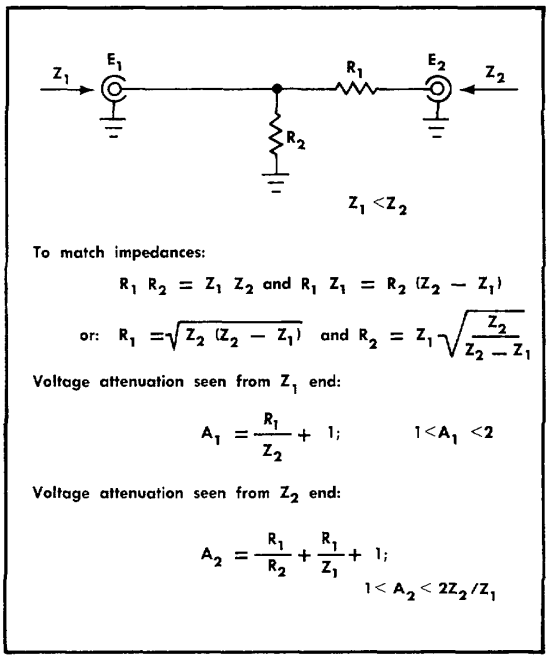

Fig. 4-3. Sample resistive impedance-matching network providing minimum attenuation.

If a low-impedance load (<50 ohms) were to be encountered, the 50-ohm pulse source would be the Z_2 source. If the load impedance were to approach 0 ohms, the value of R_1 would then approach the load impedance (low R). Voltage attenuation in this case would become quite significant:

$$\text{Attenuation} = \frac{2Z_2}{Z_L} = \frac{100}{Z_L} \text{ (very high)}$$

The illustrated network can be modified to provide different attenuation ratios by adding another resistor (<R_1) in series between Z_1 and the junction of R_1 and R_2.

Probes

For relatively high-impedance measurements of nanosecond signals, special passive or cathode-follower signal probes are available for use with the Type 3S1 Sampling Unit. Passive probes may also be built into or onto the circuits to be monitored, to minimize changes in loading.

Passive Probes. The Tektronix P6034 10X Probe and the P6035 100X Probe are moderate-resistance passive probes designed for use with 50-ohm systems. They are small in size, permitting measurements to be made in miniaturized circuitry. Power rating is 0.5 watts up to a frequency of 500 MHz. Momentary voltage peaks up to 500 volts can be permitted at low frequencies, but voltage derating is required at higher frequencies. Characteristic data is given in the probe instruction manuals.

The P6034 10X Probe places 500 ohms resistance and less than 0.8 pF capacitance in parallel with the signal source

at low frequencies. The probe bandwidth is DC to approximately 3.5 GHz, and risetime is 100 picoseconds or less (10% to 90%). At 1 GHz the input resistance is about 300 ohms and the capacitive reactance is about 400 ohms.

The P6035 100X Probe places 5 kΩ resistance and less than 0.7 pF capacitance in parallel with the signal source at low frequencies. Bandwidth of the probe is DC to approximately 1.5 GHz, and risetime is 200 picoseconds or less (10% to 90%). At 1 GHz the input resistance is about 2 kΩ and the capacitive reactance is about 450 ohms.

Cathode-Follower Probes. The Tektronix P6032 Cathode-Follower Probe is a high-impedance high-frequency probe for Tektronix sampling systems. Bandwidth is DC to approximately 850 MHz, and risetime is 400 picoseconds or less. Seven attenuator heads are provided, with attenuation factors from 10X to 1000X for the combination of probe and attenuator. Input resistance is 10 megohms at DC, and the parallel capacitance ranges from 1.3 pF to 3.6 pF, depending on the attenuator head used. At 1 GHz the capacitance reactance is about 100 ohms for the 10X attenuator and 2 kΩ for the 1000X attenuator.

The advantage of the cathode-follower probe is the high input resistance and low capacitive loading at moderately high frequencies. Dynamic characteristic data is given in the probe instruction manual.

Built-In Probes. Another satisfactory method of coupling fractional nanosecond signals from within a circuit is to design the circuit with a built-in 50-ohm output terminal. With the method, the circuit can be monitored without being disturbed. When the circuit is not being tested, a 50-ohm terminating resistor can be substituted for the test cable. If it is not convenient to build in a permanent 50-ohm test point, an external coupling circuit, which may be considered a probe, can be attached to the circuit.

Several factors must be considered when constructing such a built-in signal probe. A probe is designed to transfer energy from a source to a load, with controlled fidelity and attenuation. Both internal and external characteristics affect its operation. It must be able to carry a given energy level, be mechanically adaptable to the measured circuit and be equally responsive to all frequencies within the limits of the system. The probe must not load the circuit significantly or the display may not present a true representation of the circuit operation. Loading may even disrupt the operation of the circuit. When it is necessary to AC-couple the probe, the capacitor should be placed between the series resistance and the probe cable to minimize differences between the input characteristics with and without the capacitor. In this 50-ohm environment, stray capacitance to ground has a shorter and more uniform time constant than if the capacitor were placed at the signal source where the impedance is usually higher and of unknown value.

Fig. 4-4A shows the parallel method of coupling to a circuit under rest. Resistor R_S is connected in series with the 50-ohm input cable to the Type 3S1, placing R_S + 50 ohms across the impedance in the circuit. This method usually requires the use of an amplitude correction factor. In order to avoid overloading the circuit, the total resistance of R_S + 50 ohms should not be less than 5 times the impedance of the device (R_L in parallel with Z_O) requiring a 20% correction. The physical position of R_S will affect the fidelity of the coupling.

Fig. 4-4B shows the series method of coupling to a circuit. Resistor R_S plus the 50-ohm input of the Type 3S1 replaces the impedance of the circuit under test. If R_L is 50 ohms, simply substitute the 50-ohm test cable with no additional series resistance. It is best to locate R_S in the original position of R_L and to ground the coaxial cable where R_L was grounded.

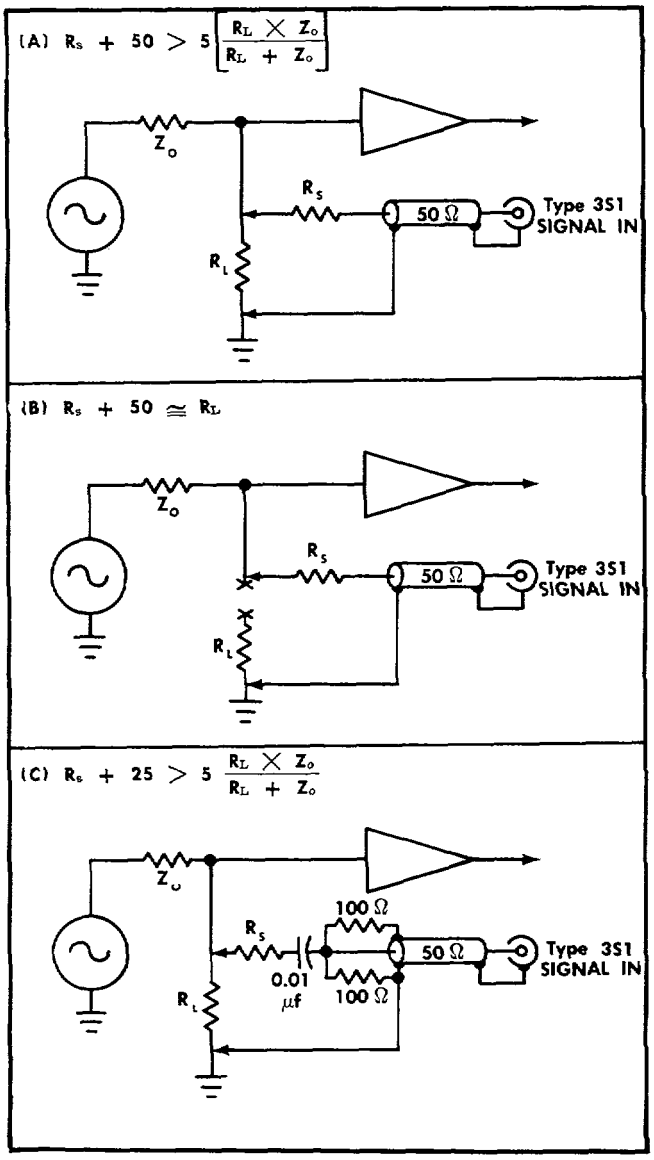

Fig. 4-4. Built-in probes for coupling to a test circuit. (A) Parallel method; (B) series method; (C) reverse-terminated parallel method.

A variation of the parallel method is the reverse-terminated network shown in Fig. 4-4C. This system may be used across any impedance up to about 200 ohms. At higher source impedances, circuit loading would require more than 20% correction. The two 100-ohm resistors across the cable input serve to reverse-terminate any small reflections due to connectors, attenuators, etc. The series capacitor, which is optional, blocks any DC component and protects the resistors.

Ⓐ

Use of DC Offset

The front-panel DC OFFSET control may be used for cancelling the effect of a DC voltage (up to ±1 volt) in the presence of a low-amplitude signal, and may be used in conjunction with the OFFSET OUT jack for making accurate DC voltage measurements of the input waveform. See information under Voltage Measurements Using the DC Offset Control earlier in this section.

In addition to providing display positioning, the DC offset for cancelling DC voltages may be used to make a particular DC level of a waveform remain stationary on the CRT screen while the mVOLTS/DIV switch is changed from one setting to another (see Fig. 4-5).

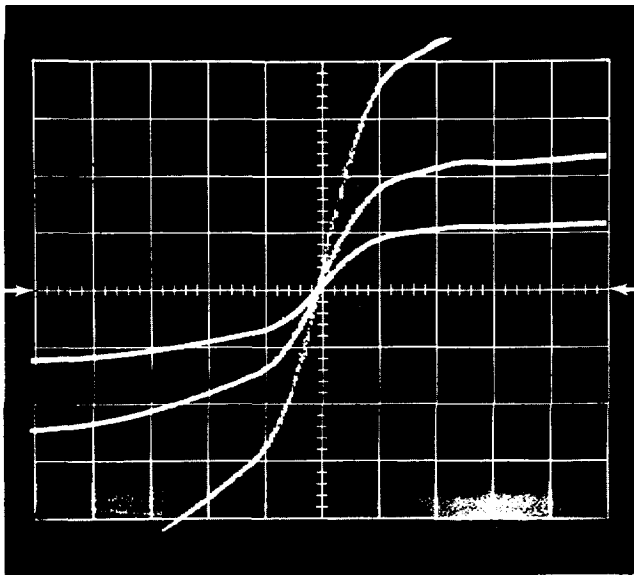

Fig. 4-5. Multiple exposure photograph showing use of DC OFFSET control for holding a particular DC level while vertical deflection factor is changed.

To adjust the DC OFFSET control for observation of a particular level of the waveform, proceed as follows:

1. Obtain a display of the input waveform in the usual manner.
2. Set the mVOLTS/DIV switch to the lowest deflection factor (highest sensitivity) to be used.
3. With the DC OFFSET control, move the selected level of the display to the graticule center horizontal line.
4. Switch the mVOLTS/DIV to the highest deflection factor to be used.
5. With the VERT POSITION control, center the selected level on the graticule center horizontal line again.
6. Repeat steps 2 through 5 for the final adjustment.

Now leave the DC OFFSET control in this final position while making observations of the display. The selected level will stay at the same vertical position on the graticule while the mVOLTS/DIV switch is rotated between its various positions. Use only the VERT POSITION control for positioning the display vertically on the graticule.

Use of Smoothing

Time and amplitude noise may sometimes be objectionable when operating at minimum deflection factors or maximum sweep rates. The SMOOTH control may be used to reduce random noise, when necessary, by decreasing the gain of the sampling feedback loop. Fig. 4-6 shows the advantage of using smoothing when observing a low-amplitude signal.

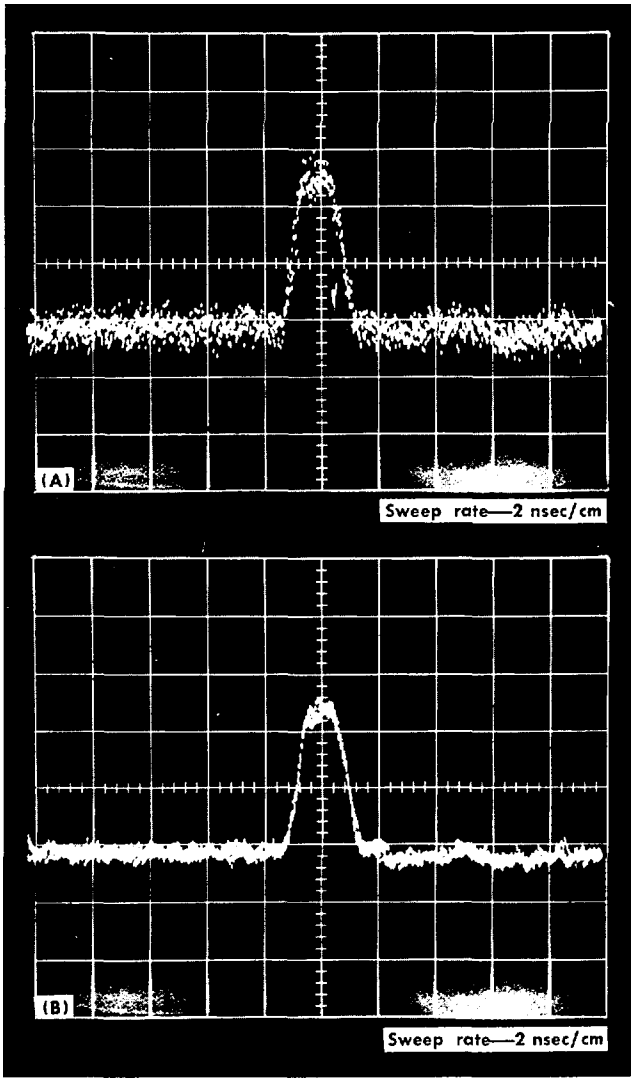

Fig. 4-6. Use of SMOOTH-NORMAL switch for decreasing display noise when viewing a low-amplitude signal. Displayed waveform is a 5-mV 2-ns pulse. (A) SMOOTH-NORMAL switch at NORMAL; (B) SMOOTH-NORMAL switch at SMOOTH.

Normally the SMOOTH position of the switch will not significantly affect the risetime of the display if the dot density is sufficient. If however, the waveform shape is affected when the switch is in the smooth position, a compromise must be made between smoothing and dot density. Fig. 4-7 illustrates the

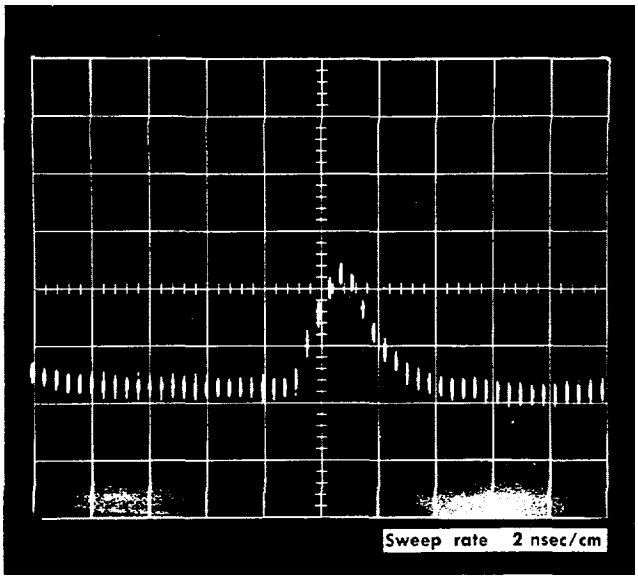

Fig. 4-7. Typical waveform illustrating the use of smoothing in conjunction with a low dot density. The waveform is the same 5-mV 2-ns pulse shown in Fig. 4-6. The distortion can be removed either by increasing the dot density or by decreasing the amount of smoothing.

effect produced by using smoothing when dot density is too low.

Selecting Display Dot Density

Selection of the dot density that will produce the best display depends on both the repetition rate of the input triggering signal, and the maximum repetition rate of the trigger circuit on the time position range being used. If the input repetition rate is low, or if the horizontal unit trigger holdoff period is long, the trace progresses very slowly across the CRT when the dot density is high. On the other hand, if the dot density is set lower than necessary, some of the display information may be unnecessarily lost between samples. In general, the best setting of the Samples/Div control in one that produces the highest dot density possible with a reasonable display repetition rate. If there are fast-rise portions on the waveform, however, it may be advantageous to set the Samples/Div control for a more dense display in order to observe the detail of the waveform.

If smoothing is used for reducing display noise, the dot density must be sufficiently high to allow the sampling circuits to follow the input signal closely. If the shape of the displayed waveform changes as the Samples/Div control is changed, the display is being modified by the combination of smoothing and low dot density. In this case, the control should be set for the best compromise between repetition rate and dot density that dose not change the display waveshape significantly from that present with a high dot density.

"False" Displays

Due to the nature of the sampling display, it is sometimes possible to obtain a waveform on the CRT screen that is not a true representation of the input signal with respect to equivalent time, if the sampling rate is very close to a sub-multiple of the signal frequency. This type of display appears as a waveform of a much lower frequency than the input signal, and is caused by sampling at such a slow rate that the samples are taken on widely-separated portions of the signal. Each sample represents the correct amplitude at the instant of sampling, but not enough samples are taken to trace out the correct waveform.

In addition, the choice of a sweep rate that is too slow may cause a false display. The false display may be detected merely by changing the dot density; i.e., changing the Samples/Div switch on the sampling sweep plug-in from 10 to 100. If the apparent timing of the display changes, the display is false. Increase the sweep with Time/Div switch on the time-base until a change in dot density from 10 to 100 does not change the apparent timing of the display. See Fig. 4-8 for on example.

Single Sweep

A single-sweep presentation of the CRT display may be obtained with the sampling sweep plug-in Display Mode switch set to the Single Sweep position. This feature may be used for viewing or photographing a waveform on a slow-moving sweep or a waveform that changes shape over a relatively short period of time.

To display a single sweep of the CRT:

1. Set the triggering controls with the Display Mode switch in the Normal position (not single sweep).
2. Now set the Display Mode to Single Sweep. The sweep will be held off following the completion of the current sweep.
3. Press the Start (or RESET) button. The sweep is then armed and the sweep will occur immediately if the triggering information is still arriving.

Real Time Sampling

In real time sampling the Type 3S1 samples the input signal at a rate of 100 kHz. By providing a real time sweep, the Type 3S1 is useful to display signals at slower sweep rates than is provided with the equivalent time bases. At a sweep rate of 0.1 ms/div, 100 samples are provided per sweep. At slower sweep rates more samples are provided per sweep as the rate is constant at 100 kHz. Other characteristics, in addition to slow sweeps at full bandwidth, are reduction of random noise in the display through smoothing, and DC offset capabilities matched with good overload recovery. Real time displays are useful with single channels, (CHAN A or B), DUAL-TRACE, and A + B operating modes.

Real time numerical voltage measurements can be made with the Type 3S1 when used with the readout system such as Tektronix Type 567 Oscilloscope with Type 6R1A and Type 3B2 or Tektronix Type 568 with Type 262 and Type 3B2. Useful modes of operation for these measurements are; CHAN A, CHAN B, and DUAL-TRACE. For a performance check of real time operation see step 20 and 21 in Section 7.

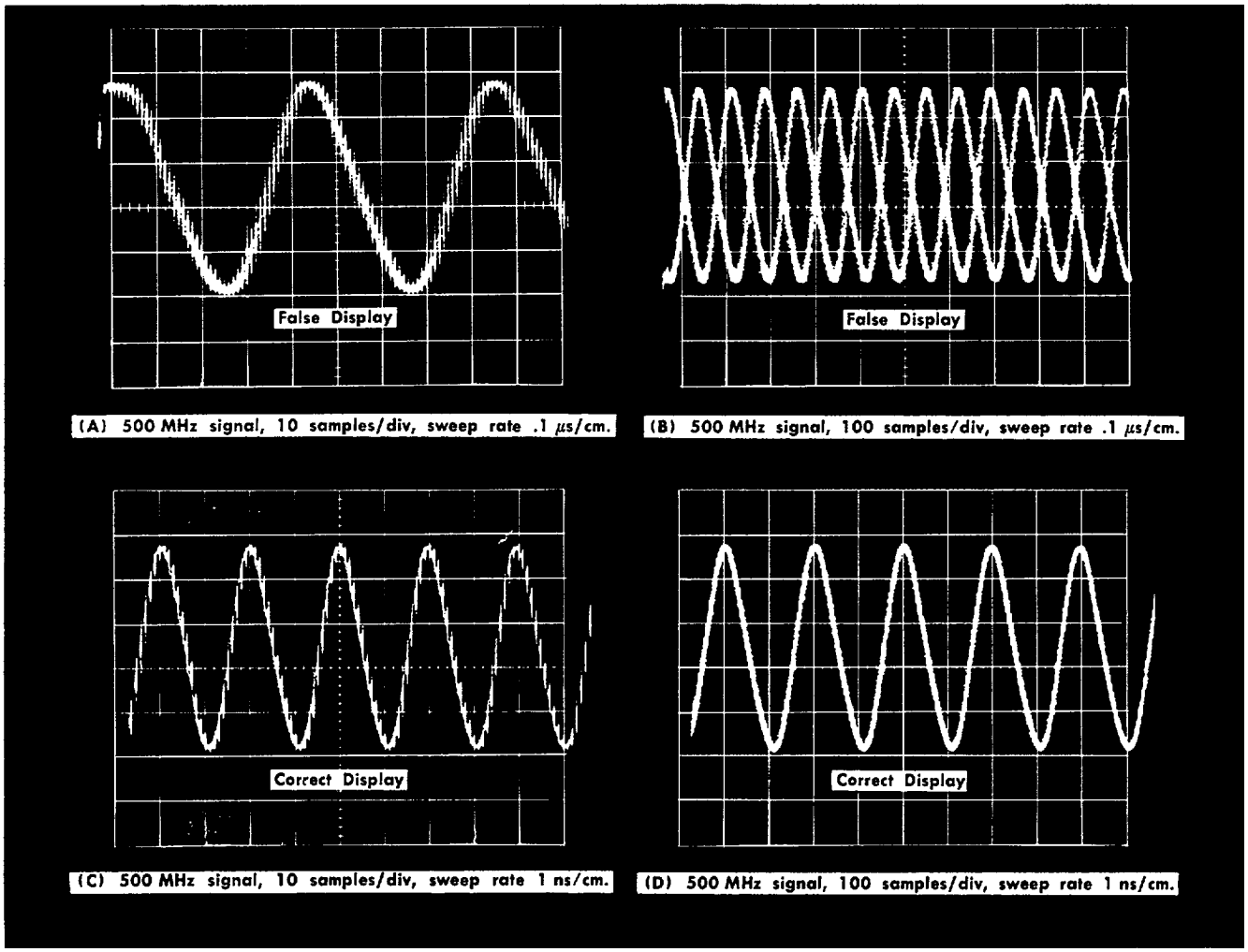

Fig. 4-8. Typical "false" sampling display showing the means of detecting and eliminating the "false" presentation. (A) 500 MHz signal, 10 samples/div, sweep rate .1 ms/cm. (B) 500 MHz signal, 100 samples/div, sweep rate .1 ms/cm. (C) 500 MHz signal, 10 samples/div, sweep rate 1 ns/cm. (D) 500 MHz signal, 100 samples/div, sweep rate 1 ns/cm.

SECTION 5
CIRCUIT DESCRIPTION

This section of the manual contains a block diagram analysis of the Type 3S1 followed by a detailed circuit description. The reader may find it helpful to refer to Basic Sampling Principles in Section 2 of this manual if the purpose of a particular circuit is not immediately clear.

BLOCK ANALYSIS

Since the A and B signal channels are identical, the block diagram discussion will be concerned only with the A channel. Refer to the diagrams at the rear of the manual for the overall block diagram.

The front panel A INPUT connector presents a 50 ohm impedance to applied signals. The signals should be from a 50 ohm source, or through suitable impedance matching networks if the source impedance is other than 50 ohms. The 50 ohm environment consists of the front panel connector, the trigger take-off, the delay line, the input to the blow-by correction circuit, and the lumped constant terminations at the sampling bridge. Taken as a composite network, they combine to make the input connector appear as a 50 ohm transmission line that is terminated in 50 ohms.

A Trigger Take-off

The trigger take-off is a resistive divider network that picks off about 12% of the voltage applied to the input connector and makes it available to the trigger selector switch. The trigger selector switch is so arranged that the trigger take-off is terminated in 50 ohms regardless of whether the trigger signal is being used or not. Therefore, changing the trigger selector switch setting does not change the 50 ohm environment for the incoming signal.

55 Nanosecond Delay Line

The portion of the applied signal not diverted by the trigger take-off circuit proceeds down a length of 50 Ω coaxial transmission line which has a transit time of 55 nanoseconds. The purpose of the line is to delay the arrival of the applied signal to the sampling gate. The delay permits the timing unit to get the sampling process started before the signal arrives at the sampling gate.

A Sampling Gate

The sampling gate consists of four special-purpose high-speed diodes connected in a bridge circuit that is normally back-biased and not conducting. The purpose of the sampling gate is to isolate the applied signal from the preamp input except for a very short interval of time. The effective sampling time duration when the Type 3S1 sampling gate is caused to conduct is about 350 picoseconds. The sampling efficiency of the bridge is about 15%. That is, the preamp input voltage changes by only 15% of the difference between its voltage level prior to sample time and the instantaneous value of the input signal at sample time.

Blow-by Correction Circuit

When the applied signals contain steep wave fronts, a small percentage of the high frequency energy couples through the capacitance of the bridge diodes when they are back biased and not conducting. This energy is called blow-by and is generally undesirable. The blow-by correction circuit inverts the applied signal and applies some of it to the output of the sampling bridge to remove the capacitively coupled and unwanted signal.

Preamplifier

The preamplifier consists of a DC-coupled operational amplifier with a time constant in the feedback path such that the amplifier has both good DC stability and high AC gain. The output of the preamp is AC coupled to the forward-gain attenuators on the mVOLTS/DIV switch. There are three inputs to the preamplifier which are effectively summed at a common input point; (a) a DC offset voltage which is manually selected by a front-panel control, (b) a DC level from the memory amplifier which was established by the previous sample, and (c) an output from the sampling bridge when the bridge is gated into conduction by the sampling strobe pulse.

The preamplifier input voltage normally resets at the sum of two DC voltages, the DC offset voltage and the DC feedback voltage from the memory amplifier. During the 350 picoseconds when the sampling gate conducts, the preamp input voltage changes towards the instantaneous voltage of the applied signal. During the period that the sampling bridge conducts, the preamp input capacitance allows the voltage to change by only about 15% of the difference between its quiescent value and the instantaneous signal value. During this short time, the signal source impedance is 25 ohms; thus the 12% factor (mentioned previously under A Trigger Take-off) is constant for all signals. Although 100% of the signal amplitude is never coupled into the preamp input, the AC Amplifier and Memory circuits feed back the equivalent of 100% of the applied signal to the preamp input. The small signal voltage at the preamplifier input and the low frequency amplifier versions of it in the AC Amplifier and Memory, are referred to as the error signal. The error signal causes a DC feedback from the memory amplifier. This feedback adjusts the preamp input voltage to the exact value of the input signal at the instant the input voltage was sampled. If smoothing is used, the error signal change to the feedback from the memory amplifier is less than enough to place the preamp input to 100% of the sampled signal. Since the output from the preamp is AC coupled, only changes in input voltage are coupled to the forward gain attenuators.

Forward-gain Attenuators

To satisfy the operational requirements that must be met, the forward-gain attenuators exist in three sections. Each section can independently change the amount the error signal is amplified before it finally affects the output of the memory amplifier. The three sections are; (a) the SMOOTH-NORMAL switch, (b) the panel-mounted A DOT RESPONSE control, and (c) the forward attenuator.

With the SMOOTH-NORMAL switch in the NORMAL position, the A DOT RESPONSE control properly calibrated, and the forward attenuator in any of its positions, the amount of gain applied to the error signal will cause the output of the memory amplifier to change by an amount that reduces the input error signal to zero as the result of only one sample. This means the memory amplifier must change by an amount to overcome the attenuation of the feedback attenuator, and still change the DC voltage fed back to the preamp input by about 6.7 times the amount of the original sampled error. This change is needed to compensate for the 15% sampling efficiency. This condition is known as unity dot response, and exists when the forward gain of the error signal amplifiers is sufficient to reduce the input error signal to zero after a single sample. (Unity dot response is required of the Type 3S1 when using random sampling with the Type 3T2 Random Sampling Sweep unit.)

SMOOTH-NORMAL Switch

The SMOOTH-NORMAL switch is a front-panel operational control which selects unity dot response in the NORMAL position, or reduces the forward gain applied to the error signal by a factor of 3 in the SMOOTH position. The purpose of the SMOOTH mode is to reduce the effect of random noise on the display with the possible compromise of slowing the displayed risetime. If the dot density is high compared to the applied risetime, the compromise is not severe. See the Type 3S1 Basic Principles Section 2 for a more complete discussion of the effects of smoothing on displayed risetime.

A DOT RESPONSE Control

The A DOT RESPONSE control is a front-panel screwdriver adjustment which affects the forward gain applied to the error signal. Its purpose is to provide a readily accessible compensation for minor dot response changes due to temperature, amplitude and time.

Forward Attenuator

The forward attenuator is mechanically ganged to the feedback attenuator. The two have the same attenuation ratios, and work inversely to each other so that the loop gain remains the some for all deflection factors chosen with the mVOLTS/DIV control.

AC Amplifier

The AC amplifier is an AC coupled operational amplifier with low impedance emitter-follower output. It provides part of the overall forward gain for the error signal and drives the memory gate and memory amplifier.

Memory Gate

The memory gate is a pulse driven diode gate that connects the output of the AC amplifier to the input of the memory amplifier while the memory gate pulse is present. At all other times it holds the input to the memory amplifier open. The memory gate starts conducting at the same time the sampling gate conducts, and continues for approximately 0.3 ms. The 0.3 ms conduction time allows the low frequency, AC coupled error signal to fully change the memory output voltage each sample. The non-conducting memory gate prevents the memory output voltage from drifting between samples.

Memory Amplifier

The memory amplifier is a high input impedance integrating operational amplifier. It stores DC equivalent of the error signal in a low-leakage capacitor and holds the memory output voltage constant between samples. It is a zero-order hold memory; that is, after a correction is stored it holds the level constant. It does not return to zero, nor does it anticipate the next correction. The output is a low-impedance emitter follower which drives the feedback attenuator, the panel mounted A OUT jack, the inverter and the INVERT-NORM selector switch.

Feedback Attenuator

The feedback attenuator establishes the ratio between the memory amplifier output and the feedback voltage applied to the sampling bridge output. It determines the deflection factor. The feedback attenuator is mechanically ganged with the forward attenuator. They have the same attenuation ratios and work inversely to each other so that the loop gain remains constant for all deflection factor settings. The feed-back attenuator is part of the front-panel mVOLTS/DIV switch. The voltage output of the feedback attenuator is applied to the preamp input and is the voltage against which the next sample will be compared. Any new voltage difference generates a new error signal.

DC Offset Circuit

The DC offset circuit is a manually variable low impedance stable DC power supply. Its range is from +10 to -10 volts DC referenced to chassis ground. 1/10 of the DC offset voltage is added to the feedback extension or vertical "windowing" of the applied signal and permits examination of small voltage segments of an input signal from +1 to -1 volt. The full DC offset voltage (ten times the offset of the signal) is available for monitoring at a front panel jack, allowing quantitative voltage measurements by the slideback technique.

Avalanche Circuit

The avalanche circuit consists of an avalanche transistor and its associated circuitry. It produces a fast-rise negative-going pulse which serves as the common coordinating signal for various pulses within the Type 3S1 sampling unit. In the TRIGGERED mode the avalanche circuit is driven by the timing unit and in turn drives the snap-off diode, the memory gate driver, and the dual-trace driver.

In the FREE RUN mode, the avalanche circuit is driven by the free running dual-trace driver.

Snap-off Circuit

The snap-off circuit consists of a snap-off diode together with its environment and shorted pulse clipping lines. The snap-off circuit is driven by the steep wave front from the avalanche circuit. The snap-off diode generates a very fast rise pulse that is cancelled after 350 picoseconds by the shorted pulse clipping lines. This 350 picosecond pulse is the interrogate strobe that gates both channel sampling bridges into conduction.

Memory Gate Driver

The memory gate driver is an overdriven common-emitter amplifier. The memory gate driver is driven by an AC coupled pulse from the avalanche circuit. It shapes a 0.3 μs pulse and drives both channel memory gates. The memory gate driver causes the memory gates to conduct at sampling time and holds them in conduction for about 0.3 μs.

Dual-Trace Driver

The dual-trace driver is an AC-coupled multivibrator that is astable for the NON-SAMPLING 2B, 3T-SERIES Sampling Mode, and monostable for the SAMPLING 3T-SERIES Sampling Mode. One side of the multi has a lumped constant tank circuit connected as a Colpitts oscillator.

In the sampling 3T-series mode, the tank circuit is shorted and the multi is monostable and operates only on a trigger from the avalanche circuit. The output of the dual-trace driver triggers the dual-trace multi in the dual-trace mode of operation and blanks the CRT during sampling time (typically 2 μs). As an example, at the maximum sampling rate of 100 kHz, or 10 μs between samples, the CRT is unblanked for approximately 8 μs to display the sample.

In the non-sampling 2B, 3B-series mode, the tank circuit is not shorted and the multi oscillates at a 100 kHz rate after the fashion of a Colpitts oscillator, triggering the avalanche circuit in addition to its other outputs.

Inverter

The inverter is a DC-coupled unity gain operational amplifier. Its output is 180° out of phase with its input, with ground as the crossover point. The input to the inverter is driven by the memory amplifier output. Both polarities of the display signal are available at the INVERT-NORM switch so the operator can display the signal normally (up deflection for positive-going slopes) or inverted (up deflection for negative-going slopes). The switch does not affect the polarity of the vertical signal output at the A OUT jack.

A Channel Amplifier

The A Channel Amplifier is a DC-coupled operational amplifier. Its purpose is to amplify the memory output signal and to add display positioning by the front panel A POSITION control. The input signal has the polarity selected by the INVERT-NORM switch. The output of the A channel amplifier drives a common-base stage at the output Amplifier input. It also makes the A channel signal available to the trigger selector switch for use by real-time timing units. The A channel amplifier makes an output available at a rear-mounted connector for use by auxiliary digital equipment such as Tektronix Type 6R1A or Type 230 (1 V/div).

Dual-Trace

The dual-trace circuit includes a bistable multivibrator which is controlled by the Display Mode switch. In the dual-trace mode it is triggered by the dual-trace driver at each sample time. The output of the dual-trace multivibrator controls the channel selecting diodes in the collector circuits of the two input common-base amplifiers, and determines whether the A channel, the B channel, or both are displayed vertically.

Output Amplifier

The output amplifier is a single-input push-pull output stage using two operational amplifiers. It receives a single-ended input from the channel selecting diodes in the collector circuits of the common base amplifiers. The input to the output amplifier is either the A channel, the B channel or both, depending on the dual-trace multi. The output is push-pull, and drives the CRT vertical deflection plates and the position lamp driver circuit.

Position Lamp Driver

The position lamp driver circuit is a push-pull emitter coupled pair that share a constant-current emitter source. Each transistor base is driven from its respective vertical deflection plate lead. The transistor with the most positive base conducts all of the common emitter current and turns on the beam position lamp in its collector. The purpose of the beam position indicators is to help locate the trace when it cannot be seen on the CRT face.

CIRCUIT DESCRIPTION

50-ohm Input Environment

The front A INPUT connector presents a 50 ohm load to all input signals. The 50 ohm input environment consists of a trigger take-off circuit, a 55 ns signal delay transmission line, and several terminating lumped constants of the sampling bridge. The various series/parallel RC and LR combinations all combine to make the input connector impedance 50 ohms for all frequencies.

The trigger take-off circuit (Diagram 2) consists of a resistance divider connected directly to the input transmission line. Resistance loading of the 50-ohm input circuit reduces the input resistance by 6.727 Ω. The actual input resistance is restored to 50 Ω by a series resistor, R100. The trigger take-off resistors located just behind the input connector are R100 and R101. They feed a 50 Ω transmission line and then the INTERNAL TRIGGER switch. At the INTERNAL TRIGGER switch, about 12% of the input signal is sent to the horizontal timing unit or is terminated to ground in R103-R104, depending upon the switch position.

Termination of the trigger take-off circuit remains 50 Ω for either position of the INTERNAL TRIGGER switch. When at A (or B), the 50 Ω termination is a complex function that includes C109-R109 and L113. L113 has very low DC resistance, and is essentially not there for very high frequency signals. C109 couples very high frequency signals directly to the timing unit

50 Ω trigger circuit. DC signals "see" only R109, and essentially no resistance due to L113. This circuit assures there is always a 50 Ω termination on the trigger take-off circuit. There is no internal triggering possible from DC signals.

Components of the internal trigger circuit mounted at the instrument rear panel, C113 and T113, assure the circuit has no ringing due to step signals when the Type 3S1 is operated on an extension cable during maintenance or calibration.

Delay Line

The delay line is a length of 50 ohm coaxial transmission line with a signal propagation time of 55 nanoseconds. Its purpose is to delay the arrival of the applied signal at the sampling bridge long enough for the timing unit to trigger and start the ramps. The delay line has some high frequency distortion, called "dribble-up". The term "dribble-up" refers to medium high-frequency distortion of a step signal caused by the normal energy losses of a transmission line. See Fig. 4-2C for on example of "dribble-up'". This distortion is compensated by the lumped constant terminating network.

The DC and low-frequency 50-ohm termination for the delay line is made up of R115, R118, R119, the DC resistance of LR118 and LR119, R125 and R124. LR118 and LR119, R115, R116, C115, and C116 compensate for the delay line high frequency distortion. Time constants of these compensating elements combine to produce an impedance of 50 ohms independent of frequency.

Blow-by Correction

Input signal which is capacitively coupled to the preamplifier grid and the strobe-corners of the sampling bridge (those corners receiving the sampling strobe pulses) cause a distortion in the displayed waveform. This unwanted signal, called blow-by, is coupled primarily through the junction and mounting capacitance of the four sampling bridge diodes, at a time when the diodes are not conducting. However, since the memory gate passes signal for a much longer time than the sampling bridge (300 ns versus 0.35 ns) this blow-by signal is recognized by the memory and displayed on the CRT. Uncompensated blow-by can affect the display by several per cent.

The blow-by compensation circuit removes the blow-by signal, and at the same time uses some of it to compensate for losses in the delay line.

The input signal is attenuated by R124 and R125 to minimize input loading, and then is inverted by Q121. This inverted signal, in different amplitudes, is applied to the strobe corners through C133 and to the preamplifier input through C130. The correction signal applied through C133 is slowed by the 0.5 ms time constant of R122, R132, and C132 in order to allow a small amount of blow-by to remain at the strobe corners for a short time. This has the effect of compensating for some of the losses in the delay line. Some of this strobe-corner blow-by reaches the preamplifier input but is removed by a similarly shaped correction signal through C131.

Blow-by from input signals with transition times greater than 1 ms is not noticeable; consequently the low-frequency gain of the blow-by correction amplifier is not important. Capacitors C120 and C128 allow the inversion of 1 ms signals without attenuation.

Sampling Bridge

The sampling bridge consists of D137A, B, C, and D. Its purpose is to connect the incoming signal to the preamp. Connection occurs at the time the diodes are forward biased into conduction by the gate generator output signal that arrives through J139, T140 and T139. The signal is single-banded as it enters J139. T140 and T139 convert it to a very well balanced, push-pull pulse, which is then capacitively coupled to the two bias corners of the sampling diode bridge. R139-R140 help balance the gate generator pulse signals to be equal in respect to ground. The sampling diodes are normally back biased by the A Bridge volts from the network consisting of R190 through R199, C190 and C194. During sampling time, the strobe pulses from T139 forward bias the diodes, and current flows from the signal to the gate of Q151 (the preamp input) or vice versa, depending on the polarities involved. Q151 gate voltage changes by about 15% of the difference between it and the incoming signal during the bridge conduction time. (The AC Amplifier and Memory circuits change Q151 gate voltage to equal the sampled signal amplitude before the next sample is taken.)

DC Offset

The DC Offset supply consists primarily of Q170, Q173 and R178. The supply is a unity gain operational negative feedback amplifier with equal input and output voltages. The input impedance is high and its output impedance is less than one ohm.

Q173 base-emitter junction can be thought of as a comparator with one input from the DC OFFSET control and the other input from Q170 collector. Most of the current in R175 passes to Q170 collector through D175, with about 1 mA going through Q173 and R173. Should the voltage at the emitter of Q173 change, Q173 collector voltage will move in a direction to restore it to its original value. This regulator (feedback) action assures that the supply output voltage remains fixed in relation to Q173 input base voltage.

D175 provides temperature compensation so the supply output voltage remains stable with changes in temperature. As the temperature increases, the voltage drops across both D175 and the base-emitter junction of Q173 are reduced. Without D175, this junction voltage reduction would appear in the offset voltage. With D175, the temperature signal is canceled so the output voltage remains unchanged.

The DC Offset supply output voltage appears (attenuated about 10X by R188, R187 and other impedances to ground in parallel with R187) at the preamplifier input in the manner of a DC signal. Since the offset DC causes the next sample to have a greater than normal potential difference between the 50 Ω termination and Q151 gate lead, the sampled AC pulse is greater than normal. The greater than normal pulse causes a large AC Amplifier and Memory signal, which then returns from the memory output to cancel the DC Offset voltage at Q151 gate lead. The net result is a shift in memorized signal voltage at the memory output rather than a permanent change at the preamplifier input.

Feedback Attenuator

The feedback attenuator consists of R183, R185, R186A through F, R187, and R188. The purpose is to allow the memory feedback signal to Q151 gate to be changed so that the display

amplitude will be changed for a given input signal. If the feedback is attenuated, the memory output will be greater than before, in order to change Q151 input by 100% of the sampled signal amplitude. This causes a change in the input deflection factor.

The forward gain attenuator is ganged with the feedback attenuator so the total loop gain does not change when the input deflection factor is changed.

Preamplifier

The preamplifier consists of Q151, Q156, and Q158, which amplify the error signal resulting from the sampling process and drive the forward gain attenuator.

Q151, a field-effect transistor, is connected as a source-follower for low input capacitance. Signal currents in Q151 drain drive Q156 base resulting in voltage inversion and amplification at the Q156 collector. Negative feedback through R154 to Q151 source determines the overall gain. The feedback permits high amplification of fast signals due to the ratio of R154 and R152. The charging of C152 limits the low frequency response, resulting in a bandpass amplifier. The output response to the input sample is an impulse of about 300 ns duration. DC gain is essentially unity, as set by R154, R150 and R151, which limits the output voltage swing to equal the DC memory feedback. Low output impedance to positive excursions is provided to Q156 through R155 and C161. Low output impedance to negative excursions is provided by Q158 in the following manner: under quiescent conditions, about 90 millivolts exists across R155 because of Q156 collector current. C161 is then charged to the base-emitter junction voltage drop of Q158 plus the 90 millivolts. A negative input to the preamplifier reduces Q156 current. Q156 collector current reduction is replaced by Q158 base current to keep the 90 millivolts across R155 constant. This results in Q158 conducting more heavily and pulling the output negative.

Forward Gain Attenuator

The forward loop gain attenuator consists of the NORMAL-SMOOTH switch, the DOT RESPONSE potentiometer, and the mVOLTS/DIV attenuator switch.

The purpose of the NORMAL-SMOOTH switch is as follows: in the NORMAL position, the loop gain is sufficient to amplify the 15% sample and feed back a level to the preamp grid that equals the voltage to the input to the sampling bridge. In the SMOOTH position, the forward loop gain is reduced by a factor of

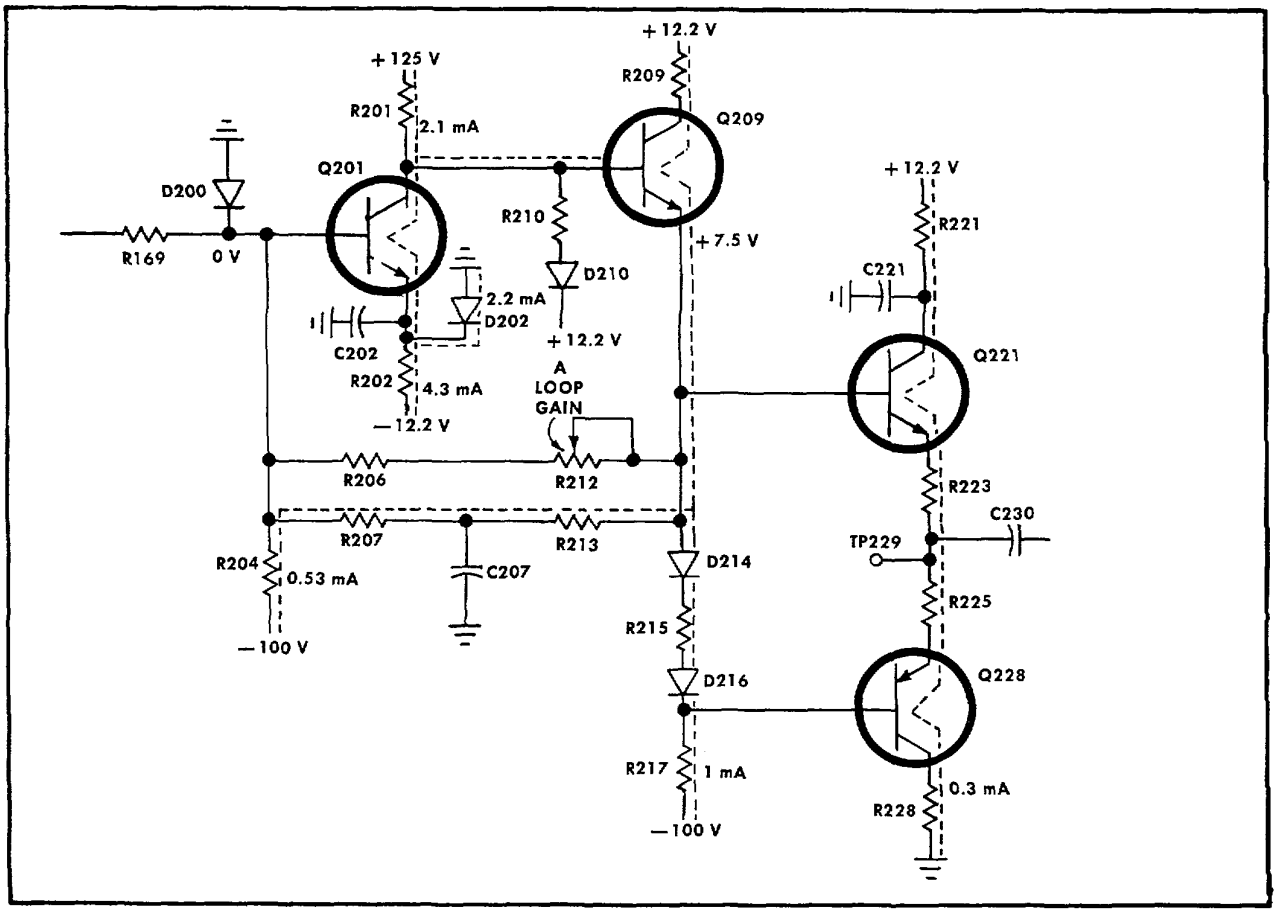

Fig. 5-1. AC Amplifier circuit, showing typical quiescent voltages and currents.

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3.3 so that several samples are required to bring the feedback voltage up to the input signal at the front of the bridge. Random noise reduction is thus accomplished. If the dot density is high, the waveform will not suffer risetime degradation.

The DOT RESPONSE potentiometer allows for adjustment of the loop gain so that the voltage feedback to the preamp input with one sample (with the SMOOTH-NORMAL switch in the NORMAL position) will just equal the signal at the input to the sampling bridge.

The mVOLTS/DIV attenuator switch changes the forward gain of the loop inversely as the feedback is changed so the dot response will remain the same on all deflection factor settings.

To establish a fixed time constant between C162 and the attenuator resistors, the input to the attenuator is always about 1 kΩ.

AC Amplifier

The AC Amplifier consists of Q201, Q209, Q228, Q221 and their associated components. (See Fig. 5-1 and Diagram 3.) Its purpose is to charge the output capacitor, C230, inversely proportional to the input signal applied to R169. The configuration is a DC-coupled phase-inverting operational amplifier with an AC voltage gain of approximately 45. The DC voltage gain is intentionally attenuated.

R202 conducts 4.5 mA from the -12.2 volt supply to ground through D202. This places the emitter of Q201 at a junction voltage drop below ground, (-0.6 volt). In the quiescent condition, with no input signal current through R169, the base of Q201 is at 0 volts. A 0.53 mA current path exists from the -100 volt supply through R204, through the series-parallel combination of R206, R212, R207 and R213, through Q209 and through R209 to the +12.2 volt supply. The voltages that result from this current place the base of Q201 at 0 volts and the emitter of Q209 at +7.5 volts (the series-parallel combination is about 13 kΩ). R201 provides 2.1 mA from the +125 volt supply to be divided between base current for Q209 and collector current for Q201. Excessive base current in Q209 will cause its emitter to pull up about the +7.5 volt level and will provide forward base current to Q201 through the feedback divider. This forward base current in Q201 will result in collector current that diverts some of the base current from Q209. The action of the DC feedback loop is to divide the 2.1 mA of current supplied by R201 between base current for Q209 and collector current for Q201 so that the emitter of Q209 is at +7.5 volts and the base of Q201 is at ground.

About 1 mA of current between the -100 volt supply through R217, D216, R215, D214, Q209, and R209 to the +12.2 volts supply establishes the voltage levels of +6.3 volts for the base of Q228, and +7.5 volts for the base of Q221. Allowing about 0.6 volt each for the base-emitter voltage drops of Q228 and Q221, this places the junction of R223 and R225 at 6.9 volts. The current (through the complementary output emitter followers) is 0.3 mA between ground in R228, Q228, R225, R223, Q221, and R221 to the +12.2 volt supply.

A positive-going signal at the input to R169 provides base current to Q201. Since the current supplied by R201 is nearly constant, the increase in collector current in Q201 divert some base current from Q209 causing its emitter to drop below its quiescent level of +5.6 volts. The drop in emitter voltage of Q209 reduces the current in the feedback resistors, R206 and R212, allowing some of the 0.53 mA from R204 to be available to cancel the input current from R169.

In the case of a negative going signal applied to R169, the signal current reduces conduction in Q201, making available more base current for Q209. The increase in base current in Q209 causes its emitter to pull up and increase the current through the feedback resistors, R206 and R212. Since the 0.53 mA from R204 is constant, the increased current through the feedback resistors cancels the negative-going signal current in R169.

Because of the action described, up to the gain capabilities of the amplifier, the emitter of Q209 will cause the current in the feedback resistors, R206 and R212, to change by an amount equal and opposite to input current provided by R169. Since the series combination of R206 and R212 (with R212 centered) is approximately 45 kΩ, and the input resistor R169 is 1 kΩ, the voltage swing at the emitter of Q209 will be 45 times greater than the input voltage to R169.

When the emitter of Q209 goes in a positive direction, forward base current is supplied to Q221. Q221 acts as an emitter follower and charges C230 through the low impedance path of R223.

When the emitter of Q209 goes in a negative direction, current through R217 provides forward base current for Q228. Q228 acts as an emitter follower to discharge C230 through the low impedance path of R225.

R202, C202, and D202 constitute a low impedance voltage reference point for the emitter of Q201. The 4.3 mA supplied by R202 is divided between emitter current for Q201 and forward bias for D202. The emitter current for Q201 is constant at about 2.1 mA; therefore the range of conduction for D202 is 2.2 mA. Its dynamic impedance for this current is about 10 Ω. C202 together with the dynamic impedance of D202 provides a by-pass time constant of about 10 μs for the emitter of Q201 to increase the high frequency gain of Q201. The voltage drop across D202 changes with temperature in the same manner as the base-emitter voltage drop of Q201, thus effectively referencing the base of Q201 to 0 volts over a wide range of operating temperatures.

The series-parallel combination of R206, R212, R207, and R213 is about 13 kΩ (depending on the setting of the LOOP GAIN control) and constitutes the DC feedback resistance for the operational amplifier. R207 and R213 are effectively by-passed by C207 for frequencies above about 1 kHz. Therefore the AC feedback resistors are R206 and R212, about 45 kΩ (again, depending on the setting of the LOOP GAIN control).

D210 and R210 make up a protective clamp circuit to limit the positive excursion of the base of Q209 to not more than +12.8 volts if a large negative signal cut off 0201, or if Q201 fails or is removed from its socket. During normal operation D210 is reverse biased and does not contribute to the function of the circuit.

D214 and D216 have temperature coefficients similar to the base-emitter voltage drops of Q221 and Q228. They serve to compensate for bias changes to Q221 and Q228 over a wide range of operating temperatures.

R221 and C221 make up a decoupling network to provide AC isolation between the complementary emitter follower pair and the +12.2 volt supply. R228 prevents oscillations by Q228.

The LOOP GAIN adjustment, R212, changes the feedback resistance and therefore the voltage gain of the amplifier. The proper adjustment of R212 is covered in the calibration procedure.

Memory Gate

The Memory Gate circuit is a pulse-driven diode gate that transfers a charge from C230 to the memory capacitor, C276. The charge that is transferred is supplied by the AC Amplifier circuitry (see Fig. 5-2).

The Memory Gate Driver provides the pulse that operates the memory gate. Quiescent circuit conditions are such that the gate diodes are back biased 5 volts by a floating Zener diode. 3 mA of current path from the -12.2 volt supply; the current divides so that 1 mA is in R233 and R232, and 2 mA in the Zener diode, D231; R231 conducts the 3 mA to the +12.2 volt supply. The voltage levels that result from this current set the top of the Zener diode at +2.5 volts and the bottom at -2.5 volts. The 5-volt drop across D231 is applied through the windings of T235 as back bias to D236, D237, D238, and D239. The junction of D237 and D239 is a high impedance point which is held at 0 volts by the Memory Operational Amplifier.

The memory gating pulse to T235 primary starts coincident with the strobe pulse to the sampling bridge and lasts for approximately 0.3 ms. The two secondary windings forward bias D236, D237, D238, and D239. The polarity of the secondaries is oriented to apply a positive voltage to the anode of D238 and a negative voltage to the cathode of D236. The four conducting diodes connect C230 to the memory amplifier input. Any AC amplifier signal current into C230 is now coupled directly to the memory amplifier input.

After the memory gate pulse terminates, the voltage drop across D231 again back biases D236, D237, D238, and D239. When the AC Amplifier returns to its normal level, C230 charges (or discharges as the case may be) back to its quiescent level through a time constant of approximately 0.7 ms formed by C230, R231, R232, R233, and R234.

D232 and D233 are clamps to prevent the memory gate diodes from being forward biased by the AC amplifier output itself. Such an output, which arrives after the memory gating pulse has ended, can be caused by the memory feedback exciting the preamplifier and AC amplifier. In normal operation they are back biased and do not contribute to the operation of the circuit.

R236, R238, and D234 are shunt damping loads to T235 to minimize inductive ringing when the memory gate driver pulse terminates. D236 and D238 are fast turn-off diodes to stop the current immediately at the end of the memory gate. D237 and D239 are low leakage diodes to prevent the gate circuit from changing the charge on C276 (in the memory amplifier feedback loop) when sampling at low repetition rates.

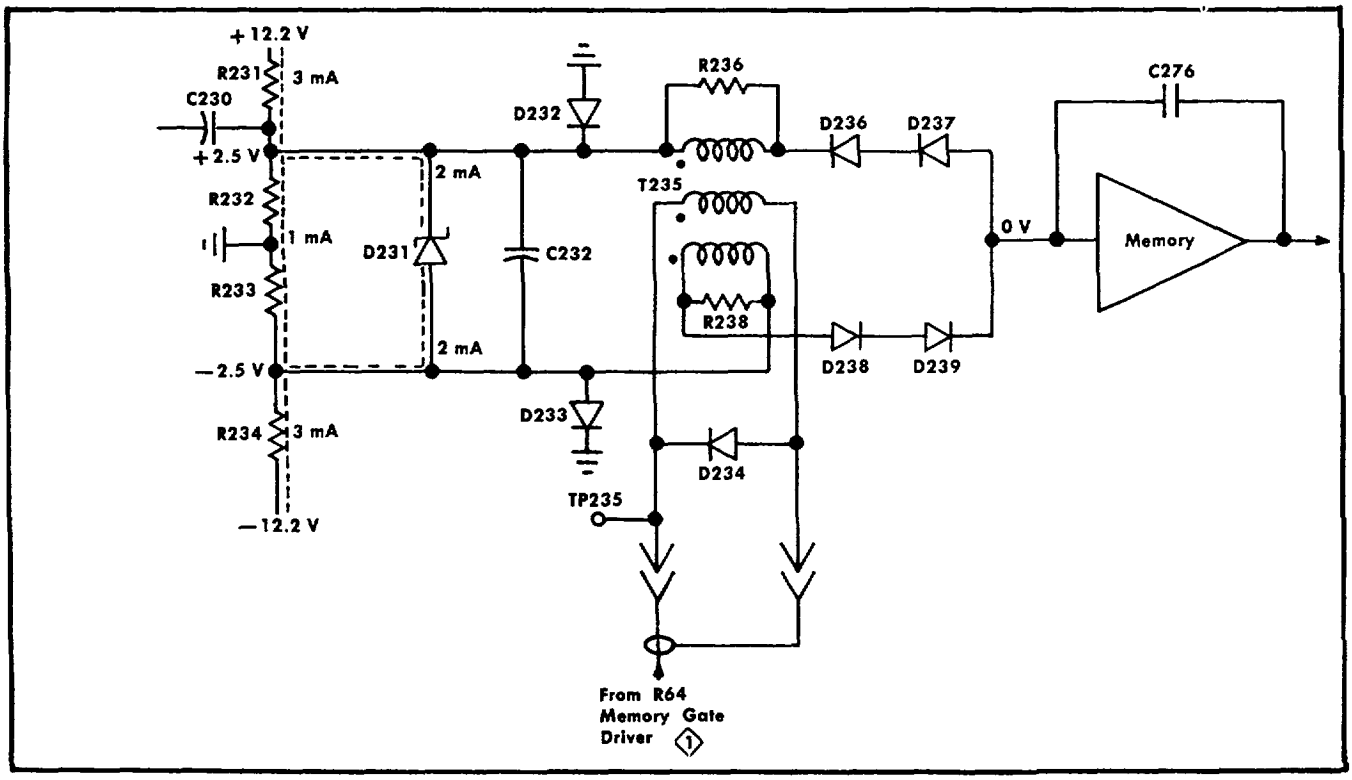

Fig. 5-2. Quiescent condition, Memory Gate circuit.

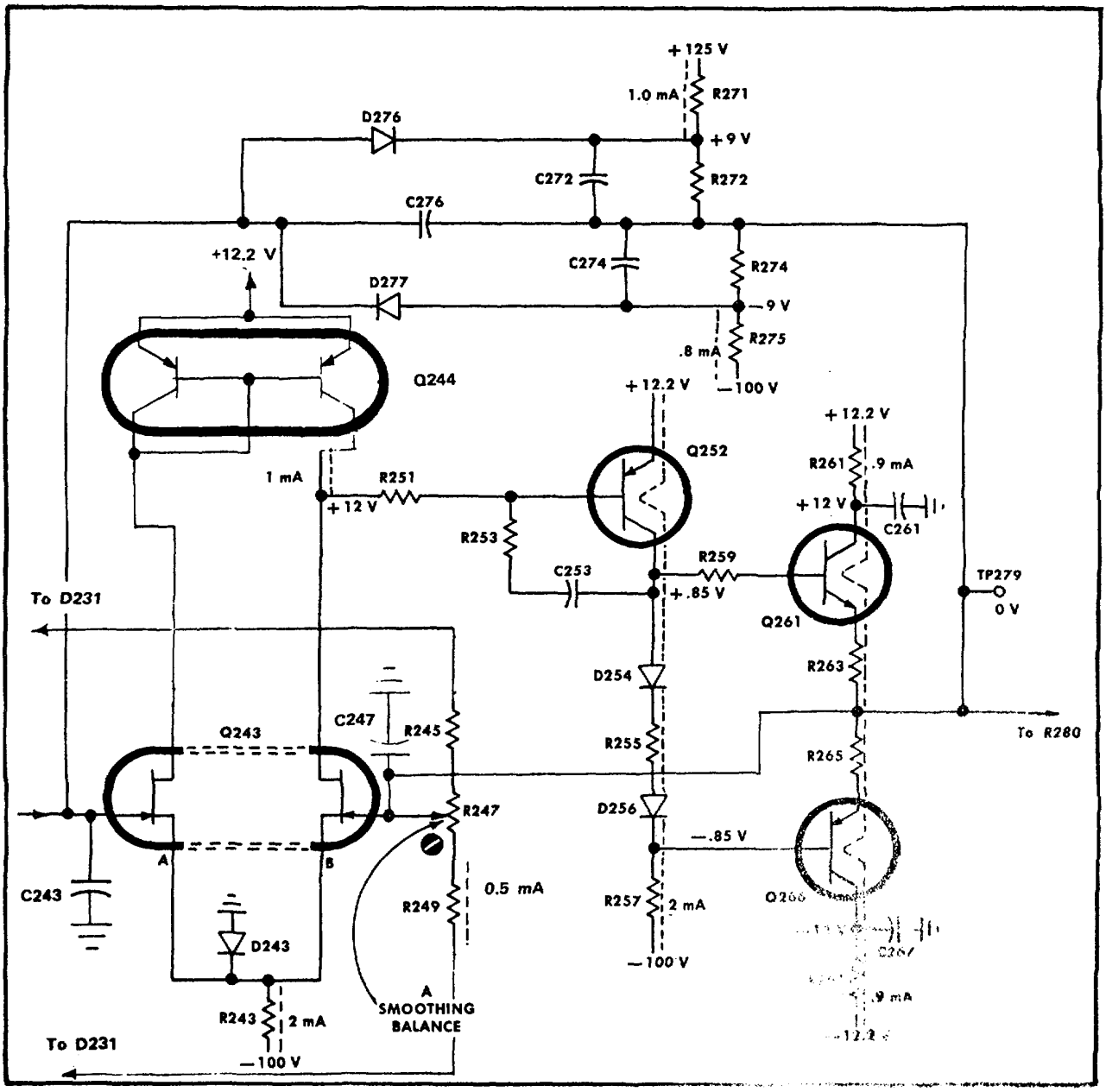

Fig. 5-3. Quiescent conditions and current paths, Memory Amplifier.

Memory Amplifier

The purpose of the memory amplifier is to store the amplified error signal until the next sample, provide an output through the feedback attenuator to the sampling bridge as a comparison level for the next sample, and provide a vertical display level to the vertical signal output and to the vertical channel of the oscilloscope (see Fig. 5-3).

The memory amplifier consists of Q243, Q252, Q261, Q266, and their associated components. It is an unusually high input impedance, low output impedance, integrating operational amplifier. The proper operation of the memory amplifier depends on the isolation at the feedback capacitor, C276; no charge or discharge path is provided other than through the memory gate, and then only when the memory gate is turned on by a pulse from the memory gate driver. D276 and D277 are low leakage diodes, the output from the memory gate is through two low leakage diodes, and the input to the memory amplifier is a dual N channel junction field effect transistor (Q243) with a very high input impedance. Therefore, C276 can be considered as a voltage source during the time interval between samples.

The input is to the gate of one of a pair of source-coupled FETs, Q243. The output of the FET pair is amplified by the transistor amplifier, Q252. The output section is a complementary pair of emitter followers, Q261 and Q266. Feedback around the integrating operational amplifier is a 160 pF capacitor, C276.

With no charge on C276, and no input, the quiescent condition of the memory amplifier is as follows:

2 mA in R243 is about equally divided between the sources of the FET pair Q243. The division is approximately equal with about 1 mA of drain current for each half of Q243. One half of Q244 conducts a constant 1 mA to the +12.2-volt supply. The drain of Q243B is held within about .5 volt of the +12.2-volt supply by forward conduction of the base-emitter junction of Q252.

The series resistors R245, R247, and R249 are connected across D231 allowing a 0.5 mA of current to flow thru R247. The Smoothing Balance control, R247, has a voltage drop of 0.5 volt centered around ground. The gate voltage for Q243B is between +0.25 and -0.25 volt depending on the setting of the Smoothing Balance control.

R257 supplies 2 mA from the -100 volt supply through D256, R255, D254, and Q252 to the +12.2 volt supply. The resulting voltage levels place the base of Q266 at about -0.85 volts and the base of Q261 at about +0.85 volts. The complementary emitter follower pair, Q266 and Q261 conducts about 2 mA from the -12.2 volt supply to the +12.2 volt supply through R267, R265, R263, and R261. Equal conduction of Q261 and Q266 places the junction of R263 and R265 at 0 volts.

The divider formed by R271, R272, R274, and R275 conducts about 09 mA from the -100 volt supply to the +125 volt supply, placing about a 9 volt charge each on C272 and C274.

During memory gate pulse time, the output from the AC Amplifier is connected to the input gate of Q243. An input voltage other than ground changes the conduction of Q243A. Since the two halves of Q243 share a total of 2 mA from the constant current long-tail resistor R243, a change in conduction of the left hand half of the FET pair results in an equal and opposite change in conduction of the right hand half. Drain current from Q243B divides between forward base current for Q252 and current through Q244B to the +12.2V volt supply. The current through Q244B is a constant 1 mA, therefore any change in drain current from Q243B is a change in forward base current of Q252.

An increase in the collector current of Q252 will provide forward base current for Q261, charging C276 in a positive direction through the low impedance path of R263 and Q261 to the +12.2 volt supply. A decrease in the collector current of Q252 will divert part of the constant 2 mA from R257 into the base of Q266, charging C276 in a negative direction through the low impedance path of R265 and Q266 to the -12.2 volt supply. The overall action of the Memory Amplifiers is to apply any input current (positive or negative) as a charge on C276, and hold the gate of the input FET very close to 0 volts.

R241 and C241 comprise a decoupling network to provide AC isolation between the input FET and the +12.2 volt supply. D243 is a protective clamp that prevents the source leads of Q243 from going more negative than -0.6 volt, permitting Q243 to be withdrawn from its socket without turning the power off. D243 is normally reverse biased and does not conduct. R251, R253, and C253 are damping components to inhibit Q252 from high frequency oscillation.

D254 and D256 have junction drop temperature coefficients similar to the temperature coefficients of the base-emitter junctions of Q261 and Q266. The diodes minimize the effects of bias changes on Q261 and Q266 over a wide range of operating temperatures. R261, C261, R267, and C267 are decoupling networks that provide AC isolation between the complementary emitter follower pair (Q261 and Q266) and the 12.2 volt power supplies. D276 and D277 are protective clamps to limit the charge on C276 to about ±9 volts. They are normally back biased and have very low leakage in the back direction. In the absence of excessive charge on C276 they do not contribute to the operation of the circuit. C272 and C274 provide a short time-constant discharge path for C276 if its charge exceeds the limits established by D276 or D277.

The Smoothing Balance control sets the DC level of the common sources of the FET pair, thereby establishing the zero signal level for the input. Its function is to compensate for DC trace shift when the smoothing selector switch is changed from SMOOTH to NORMAL.

The use of a source-coupled FET such as Q243 minimizes the effect of drain current changes due to changes in operating temperature.

Both positive and negative AC Amplifier outputs produce a current which divides almost equally through both secondary windings of T235. This current reinforces the memory gate drive current in one pair of diodes and subtracts from it in the other pair of diodes, but does not turn either pair of diodes off. This current lasts for the duration of the memory gate, and charges C276 proportional to the charge removed from C230. Since C276 is 1/6 the value of C230, the voltage charge placed on C276 will be 6 times greater than the charge removed from C230. This results in an effective voltage gain of approximately 6.

Inverter

The purpose of the inverter stage is to provide an inverted vertical display signal. The input to the stage is the level established by the Memory Amplifier. The output is to one side of the INVERT-NORM switch.

The Inverter is a DC coupled operational amplifier with a gain of one, with an adjustment to set the output level equal to zero when the input is zero. The input signal is applied to R280, and causes an error signal at the base of Q283. The error signal is amplified by Q283 and is applied to the feedback resistor R288 through the emitter follower Q288. Since the feedback resistor R288 is the same value as the input resistor R280, the signal at the emitter of Q288 is equal in amplitude to the input signal and opposite in polarity. The quiescent conditions of the INVERTER with the INVERTER ZERO adjustment R283 set for zero output with zero input voltage are as follows; 0.84 mA from the -100 volt supply less the current in R282 set by R283, divides equally between R280 and R288.

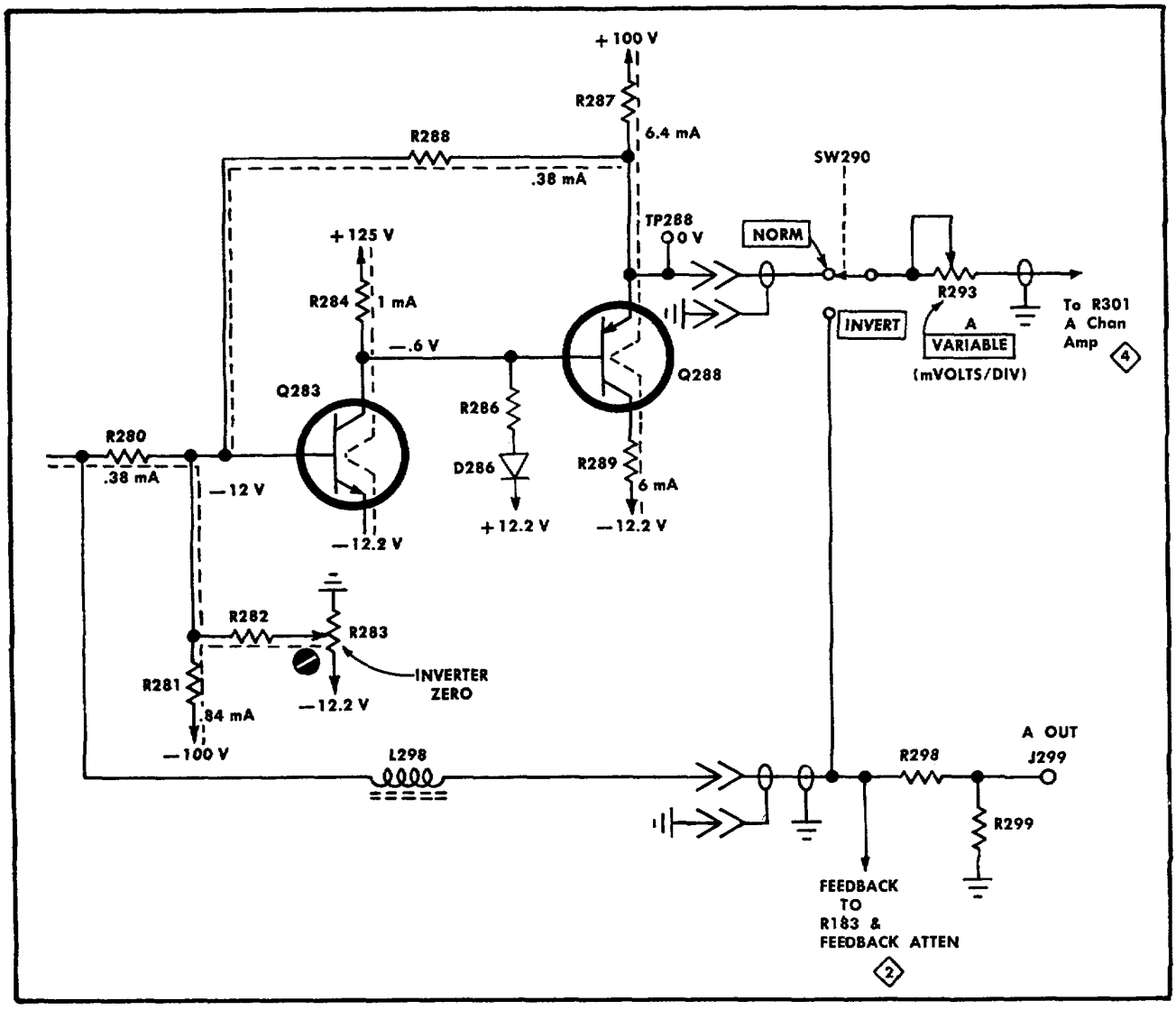

Fig. 5-4. Voltages and current paths under quiescent conditions, inverter circuit.

About 0.38 mA current path is back to the low impedance output of the Memory Amplifier through R280, and about 0.38 mA current path is through R288 and R287 to the +100 volt supply. These currents establish the base of Q283 at -11.6 volts. Q283 conducts about 1 mA through R284 to the +125 volt supply, setting its collector at 0 or slightly negative. Q288 conducts about 6 mA from the -12.2 volts supply through R287 to the +100 volt supply, holding its emitter down to 0 volts.

When a positive-going voltage is applied to the input end of R280, the increase in current in R280 provides an increase in base current for Q283. The resulting increase in collector current in Q283 increases the base current to Q288. Since R287 is longtailed to the +100 volt supply, the increase in emitter current in Q288 subtracts from the current through R288 by an amount very nearly equal to the original signal current in R280. A negative going signal applied to R280 will reduce the base current in Q283. The reduction in collector current of Q283 will reduce the base current in Q288. The reduction in emitter current from Q288 adds to the current in R288 by an amount equal to the reduction in current in R280. The action of the operational amplifier is to hold the total current in R280 and R288 equal to the current in R282 and R281. Any increase or decrease in current in R280 is accomplished by an equal and opposite change in current in R288 within the gain limitations of the amplifier. Since R280 and R288 are equal in value, this action produces a waveform at the emitter of Q288 which is equal in amplitude but opposite in polarity to the signal applied to R280. R286 and D286 make up a protective clamp which prevents destructive back bias to Q288 if Q283 fails to conduct for any reason.

R283 adjusts the DC level of the output It is used to set the output level to zero when the memory output is zero so that switching from NORM to INVERT will not cause a trace shift.

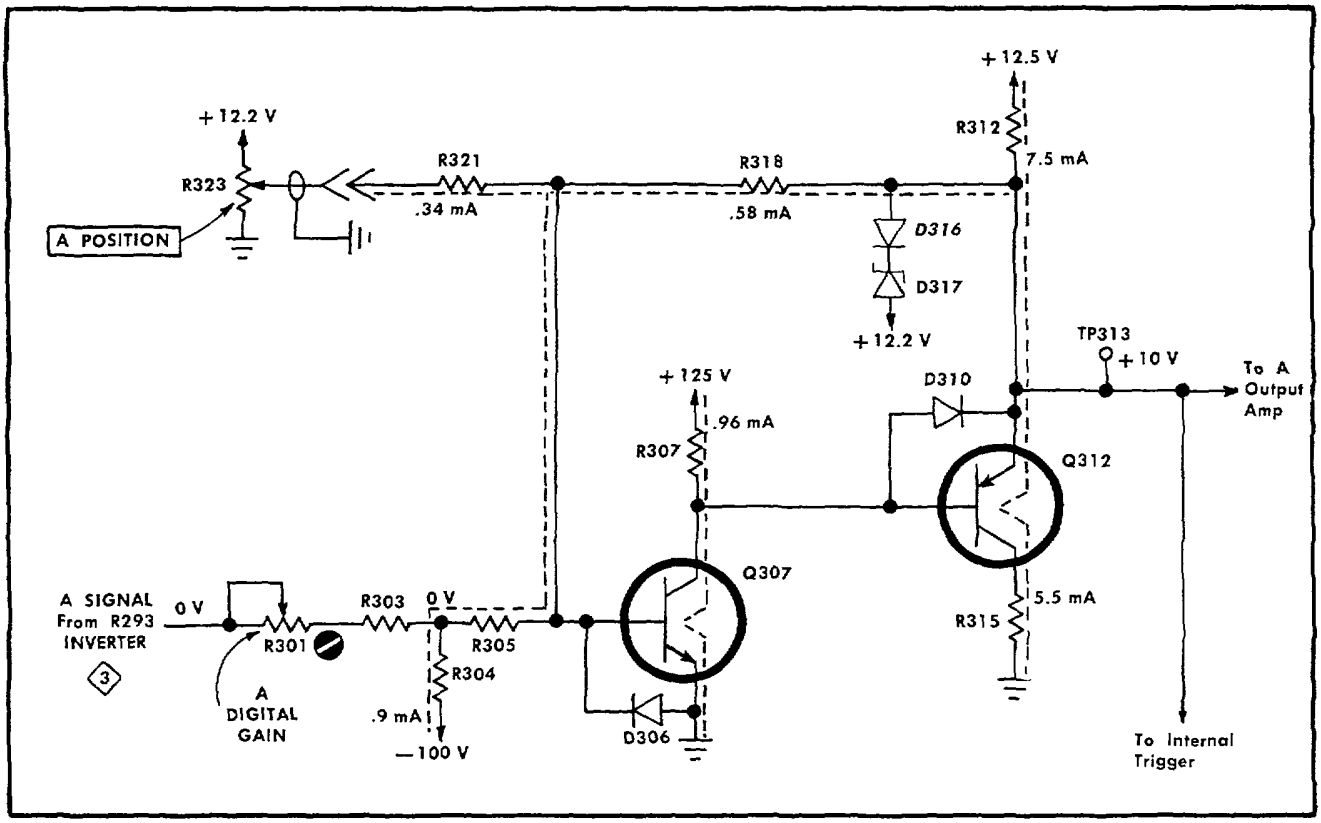

Fig. 5-5. A Channel Amplifier showing typical quiescent voltages and current with 0 volts input, +10 volts out with A POSITION control centered.

A Channel Amplifier

The Channel Amplifiers amplify the display channel signal independent of the feedback loop and add positioning voltage.

The circuit is a DC coupled operational amplifier with three current-summing inputs. The output swing is limited at ground and +19 volts. The input current summing point is referenced to one junction drop above ground.

The three current summing inputs are, (1) the A POSITION control, (2) the signal from the Memory Amplifier (through the Inverter Circuit), and (3) a low level setting bias current from the -100 volt supply.

With no input signal from the Memory Amplifier, the center voltage from the POSITION control and the bias current from the -100 volt supply will set the output level of the operational amplifier at about the middle of its permissible swing (about +10 volts). The gain from the signal input to the output is determined by the ratio of the feed-back resistance to the input resistor. The input resistance can vary from a minimum of 2 kΩ to a maximum of 14 kΩ with a nominal value of 8 kΩ when the A Digital Gain control is at center value and the VARIABLE is in the CAL position. This gives the stage a nominal signal gain of about 2 with adjustment to vary it between the limits of 1.2 and 8. The Position control can swing the output level (with zero signal in) from +4 volts to +16 volts.

The operation of the B channel amplifier is the same as described for the A channel amplifier.

Dual Trace Multivibrator

The purpose of the dual trace multivibrator is to select either Channel A or Channel B for display. See Fig. 5-6 and Diagram 7.

The circuit is a bistable multivibrator with the output voltage level either ground or +11 volts. The circuit includes Q714, Q724, and associated circuit components.

The waveform into the anode of D701 is basically a square wave, with the upper excursion limited to ground by Q38. Therefore, D701 can conduct input triggers only when its cathode is returned to some negative voltage; i.e., when the Vertical Mode switch is in the DUAL-TRACE position. In this position, R701 and R703 set the average voltage of the cathode of D701 to -12.2 volts. In all other positions of the Mode switch the cathode is returned to ground and the diode does not conduct The dual trace signal charges C702 causing a positive impulse of current to be coupled through D70, (or D706) to the collector of the “off" transistor (the collector of the "on" section of the multivibrator is at +11 volts and the coupling diode is back biased), coupled through the speed-up capacitor C719 (or C729, depending on the state of the multivibrator) and cuts off the conducting transistor. Normal multivibrator transition occurs.

In other positions of the Vertical Mode switch, the emitter of one or the other transistor is at ground, or in the A + B position both are at ground. When Q714 is not conducting, B channel

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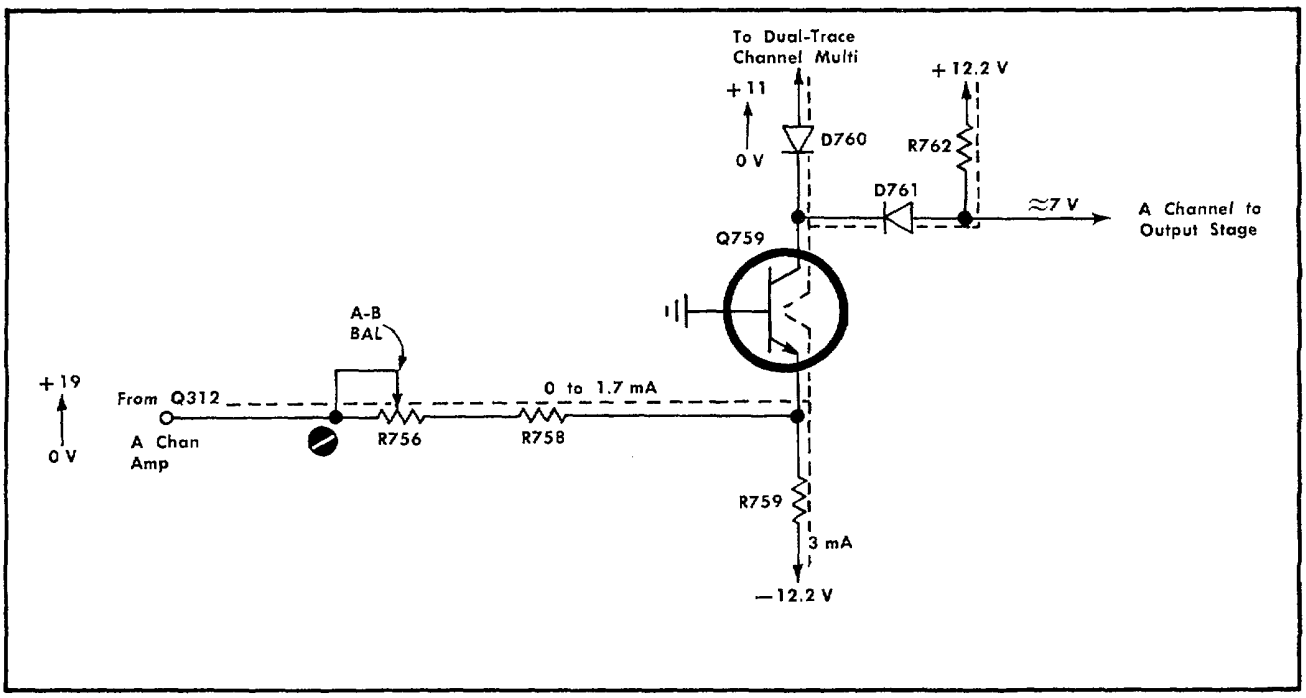


Fig. 5-6. Circuit to supply constant current during channel switching. Measurements will depend on the state of the Dual-Channel Multivibrator and the signal current.

is displayed; when Q724 is not conducting, Channel A is displayed. An output from the collector of Q714 is taken to interconnecting plug P12 pin 11 for use by the Digital Readout Unit (Tektronix Type 6R1A or 230).

Q759 provides constant current during channel switching. (See Fig. 5-6.) The circuit consists of Q759, signal gate diodes D750, D751, D760, and D761, together with associated resistors. The purpose is to steer signal current into the display channel output stage, or to divert it, depending on the state of the dual-channel multivibrator. R759 provides 3 mA from the -12.2 volt supply to be divided between emitter current for Q759 and current back to the signal source (display channel amplifier). Since the signal voltage can vary between 0 and +19 volts, and the signal path impedance is 11.5 kΩ (R756 and R758), signal current will vary from 0 to 1.7 mA. Emitter current for Q759 is the rest of the 3 mA (3 -I_{sig}), Q759 will conduct between 1.3 and 3 mA depending on the signal current.

When the A channel signal is to be displayed, the anode of D760 is a ground (dual trace channel multivibrator) and collector current path for Q759 is through D761 and R762 to the +12.2 volt supply (anode voltage for D761 is approximately +7 volts).

When the A channel is not to be displayed the anode voltage of D760 is +12 volts. Collector current path for Q759 is through D760, through the dual trace multivibrator to the +12.2 volt supply. D761 is back biased and does not conduct.

In the A + B position of the mode switch neither multivibrator transistor conducts. Both D760 anode and D750 anode are at ground. The collector current of Q760 and Q749 have a common collector load of R762 and R753 in parallel, combining both signals. The signal to the output amplifier will be the algebraic sum of A and B signals.

Phase Inverter and Output Amplifier

The purpose of the circuit is to amplify the vertical signal, convert it to push-pull, and drive the CRT deflection plates. The input receives its signal from the A channel/B channel steering network, and the output drives the CRT deflection plates and the beam position indicator neons.

The output amplifier section consists of Q771 and Q775, together with associated resistors. The circuit is an operational amplifier, with R777 as the feedback element. Gain is determined by R777/R758/R756, and by the current division controlled by VERT GAIN R764. Gain can be varied from 9 to 13 by means of the VERT GAIN control.

The phase inverter section is composed of Q781 and Q785, plus associated resistors. The circuit is also an operational amplifier, with R779 as an input impedance of 160 kΩ, and a feedback element R789, also 160 kΩ. Any change at the input (the lower CRT deflection plate) will result in on equal and opposite change at the output (the upper CRT deflection plate), as the amplifier has a gain of 1. As the voltage at the emitter of Q775 goes up, the voltage at the emitter of Q785 goes down, holding the average of the two deflection plates at +180 volts.

Position Indicators

With the average voltage of the deflection plates at about +180 volts, the total emitter current supplied by R795 will be about 0.3 mA. If the two deflection plates are at equal voltages (+180) Q793 and Q795 will share the 0.3 mA and both lights

will be on. If either side goes higher than the other, that side will take all of the 0.3 mA turning on its neon. The other transistor will be back biased and its neon will be dark.

Avalanche Circuit

The purpose of the avalanche circuit (Diagram 1) is to generate fast-rise pulses to drive the snap-off diode, initiate the memory gate, and to trigger the dual-trace driver.

The circuit consists of avalanche transistor Q11, low impedance voltage source Q7, Avalanche Volts adjustment R5, and associated fixed components.

The input to the circuit is either a positive-going pulse from the timing unit (through J1), or from the dual-trace driver when it is in the Free Run mode. The outputs are to the snap-off diode, the memory gate driver, and the dual-trace driver. When the collector voltage of the transistor is adjusted to the critical value and the transistor base-emitter junction is forward biased, avalanche breakdown between collector and emitter occurs. The transistor then rapidly becomes a short circuit allowing the charge stored on C70 to flow through the transistor (Q11), C72, T72, and D73. The peak current around the loop is approximately 1 ampere. C10 enhances the avalanche effect in Q11 by maintaining collector-base voltage during the time the circuit is being triggered.

The Avalanche Volts adjustment R5 is set for minimum noise at the most sensitive position of the mVOLTS/DIV switch. Q7 is an emitter follower to supply the collector voltage for Q11 from a low-impedance source, so that changes in duty cycle will not affect the recharging of C70.

Snap-Off Diode and Pulse-shaping Circuit

The circuit consists of coupling capacitors C78, C79, D73, and shorted transmission lines.

In the static condition, current flow is from the -12.2 volt supply through L77, Q76, R74, half of T72, D73, the other half of T72, and L71 to ground.

The shorted transmission lines are connected to D73 and extend through J78 and J79 to the sampling gate diodes. As long as D73 is conducting in the forward direction (its normal state) the transmission line input is shorted. The pulse from the avalanche transistor, Q11, (through C70 and T72) causes a heavy current to flow in the reverse direction through D73. Inherent characteristics of D73 (snap-off diode) are that even with reverse current, the diode remains a low impedance until the stored change is cleared from it. The stored charge depletes abruptly and current through D73 stops. The self inductance of T72 tries to keep a steady state current moving but now it passes through C78/C79. The shorted stubs in parallel with the transmission lines reflect back on opposite polarity pulse from the short circuit approximately 350 ps after the initial wavefront moves down the line. The total effect is that T72 and the two shorted transmission lines generate a pulse of 350 ps duration. The + and - strobe pulses generated are push-pull, one polarity to the Channel A bridge, and the other polarity to the Channel B bridge.

Memory Gate Driver

The purpose of the Memory Gate driver circuit is to gate the A and B memory, to open the A and B memory gates coincident with the strobe to the bridges, and leave then open long enough to allow for transition time through the preamplifier and AC amplifier.

The circuit consists of Q54 and Q58, Memory Gate Width control R52, and associated components. The input signal is from the avalanche transistor, and the outputs are to the A and B memory gates.

Under quiescent conditions, Q54 is conducting with it emitter level adjustable by R52 (Memory gate width). Q51 is back biased by current through R59 and D59 through D57 and R57. The base of Q58 is at about +0.6 volts (the junction voltage drop of D59).

The negative-going pulse from the collector of Q11 is coupled to the base of Q54 through R50 and C50 saturating Q54 for about 0.8 ms. The waveform at the emitter of Q54 is a negative-going fast rise flat top with an RC time-constant decoy back to quiescent level. The amplitude is determined by the setting of R52 (Memory Gate Width). The negative going waveform from the emitter of Q54 is coupled to the anode of D57 through C56, back biasing D57 for the duration of the pulse. During the pulse time when D57 is back biased 1.2 mA from the -12.2 volt supply through R59 is forward base current for Q58. Q58 saturates and its collector moves from -12.2 volts to ground. This drives current through the primary windings of the memory gate transformers T235 and T234. The pulse ends when the timing waveform again allows D57 and D59 to turn on, which returns Q58 to the off state. The timing waveform is generated at the anode of D57 by C56 being charged towards -12.2 volts through R57. Q54 remains saturated for a longer time than the desired pulse width so that it will not affect timing. As the timing waveform passes through ground, D57 turns on and the memory gate pulse ends.

Dual-Trace Driver

The Dual-Trace Driver circuit provides switching triggers to the dual-trace multivibrator and blanking pulses to the CRT that blank memory level changes and switching transients. The circuit also serves as a master timing source in the NON-SAMPLING 2B, 3B-SERIES mode.

Q31, Q38 and associated components comprise the Dual Trace Driver. The circuit is activated by input triggers received from Avalanche transistor Q11, during strobe time. Outputs from the Dual-Trace Driver are to the Dual-Trace multivibrator, blanking pulses to the CRT cathode and, in NON-SAMPLING 2B, 3B-SERIES sampling mode, triggers to the avalanche transistors.

The circuit has two configurations; (a) in the SAMPLING 3T-SERIES mode, it is a monostable multivibrator that triggers from the avalanche transistor output (b) in the NON SAMPLING 2B, 31-SERIES mode, it is a 100 kHz Colpitts oscillator.

In the SAMPLING 3T-SERIES mode, quiescent condition are such that both transistors are cut off. When a negative going trigger from Avalanche Transistor Q11 arrives at the collector of Q31 through R14 and C14, the trigger pulse is coupled through C36 to turn on Q38. The rise in Q38 collector voltage is coupled through C41 to turn on Q31. Total regeneration follows, saturating both transistors. Sustained base current for Q38 is supplied by C35 and R35 (C36 charges rapidly). Pulse width is determined by the time constant of C35 and R35. When C35 has charged, base current in Q38 drops below saturation

and the collector falls. The drop in Q38 collector voltage is coupled through C41 to reduce conduction in Q31. The rise in the collector voltage of Q31 is coupled through C36 to reduce conduction in Q38. Total regeneration follows to push both transistors into cutoff.

In the case of the NON-SAMPLING 2B, 3B-SERIES mode, SW110B, the HORIZ PLUG-IN switch, removes the short from the tank circuit and prevents the -12.2 volt supply from holding Q31 cut off. Q31 now is normally conducting, with a base current path through R27, L24, and R22 to ground. C27 and C26 together with L24 make up a 100 kHz tank circuit with drive applied from the emitter to the junction of C26 and C27. The amplitude of oscillation in the tank drives Q31 alternately into saturation and beyond cutoff, which in turn drives Q38 into saturation and cutoff. The collector waveform for Q38 is essentially a square wave at the top (most positive) position. Thus, it blanks the CRT, and switches the dual trace multivibrator. To understand the operation of the dual trace multivibrator, it is important to note that the collector of Q38 never goes more positive than ground.

Part of the base signal from Q31 is coupled through C15 to T12 to trigger the avalanche transistor in the NON-SAMPLING 2B, 3B-SERIES mode. In the SAMPLING 3T-SERIES mode (Sampling Mode switch) the pulse has no effect because the avalanche transistor is already in a state of avalanche.

SAMPLING MODE Switch

The Horiz Plug-In switch SW110B has two positions, SAMPLING 3T-SERIES and NON-SAMPLING 2B, 3B SERIES.

In the NON-SAMPLING 2B, 3B SERIES position, it allows the Dual-Trace Driver to free run, while in the SAMPLING 3T-SERIES position it prepares the Dual-Trace Driver for triggered operation as previously mentioned. In the NON-SAMPLING 2B, 3B SERIES position, the switch also couples channel output amplifier A or B (as selected by the Internal Trigger switch SW110B) to the output connector Pin 11. This is coupled in the oscilloscope to the timing unit for internal real-time triggering. In the SAMPLING 3T-SERIES position, the switch connects the output of Channel B through R641 to Pin 11 of the output connector (provided the Vertical Mode switch is in the A Vert B Horiz position). This output is useful to supply the B Channel to a sampling time base for A Vertical B Horizontal operation.

INTERNAL TRIGGER Switch

The INTERNAL TRIGGER switch SW110A (Diagram 2) has three positions A, OFF and B positions. One section selects the trigger signal from the Chan A or Chan B Trigger Take-off. In A position, the switch selects the trigger signal from R101 in the Chan A Trigger Take-off thru R109, shunted by C109 to Pin 4 of output connector P11. In this position, Chan B Trigger Take-off output from R401 is connected to a parallel combination (R106 and R107), effectively terminating this output while it is not in use. In B position, the trigger is selected similarly from R401 through R112 shunted by C112 to Pin 4. (Chan A trigger output from R101 being terminated by R103 and R104 in this switch position.) In the OFF position both trigger outputs from Chan A and B are terminated as above, and in addition, the 50 Ω coaxial line leading to pin 4 (Pin 3 is the shield connection) is terminated by R110 and R111.

Another section of the INTERNAL TRIGGER switch selects the reconstructed signal from either A or B Channel Amplifiers. In the A position, it connects from the emitter of Q312 through R332 (Diagram 4) through the Horiz Plug-In switch. If the Horiz Plug-In switch is in the NON-SAMPLING 2B, 3-B SERIES position, this reconstructed signal to Pin 11 is the triggering signal for real time sampling. Likewise (the output of Channel B Amplifier may be selected in the B position. In the OFF position, current in R334 and R332 sets the output voltage at the junction of these two resistors at -10 volts. In the A or B positions, this voltage is about ±5 volts depending upon the output of the A and B Channel Amplifiers. D331 prevents excessive negative voltage being applied to the trigger circuits during switching.

Digital Logic

Digital logic connections are provided on the P12 output connectors. Outputs are provided to handle information to the digital equipment such as Tektronix Type 568/230 or 567/6R1A combinations.

A and B signals are provided from the A and B Output Amplifiers at 1 V/div. Digital Switching pulses are provided from the Dual-Trace Multivibrator. Switching contact closures mechanically connected to the mV/DIV switches of Channel A and B conveys the switch positions when properly connected to the digital equipment.

Power Supplies

The Type 3S1 contains +12.2 and +100 volt electronically regulated power supplies. See Diagram 6.

+12.2 Volt Supply. 6.3 volts AC entering the Type 3S1 through P11 pins 1 and 2 supplies power to the primary of T820. T820 secondary provides power to the full-wave bridge rectifier D821 A, B, C, and D, producing about 20 volts DC across C822.

The regulator circuit consists of a comparator amplifier Q825, an emitter follower Q835, and series regulator transistor Q839. Q825 compares the voltage from the divider consisting of R831, R833 and adjustment (for +12.2 volts) R832, with the zener diode D827. Collector current of Q825 through D827 and R825 provides a voltage for the base of Q835 emitter follower. Q835 emitter drives Q839 series regulator. R827 provides current for D827. R829 provides current for temperature compensating diode D829. C828 is used to prevent high frequency oscillations. C839 helps to reduce the supply high frequency output impedance.

+100 Volt Supply. +125 volts from the oscilloscope entering the Type 3S1 through P11 pin 15 provides power for emitter followers Q815 and Q817. Q815 emitter supplies +100 volts to supply sampling bridges, and drives the base of Q817. Q817 supplies +100 volts to pin D of the Power Probe connectors on the front panel and to A and B Inverters. The base voltage of Q815 is set by a precision divider R813 and R814 connected between the +12.2 and +125 volt supplies.

R815 and R817 are series dissipation limiting resistors in the collectors of Q815 and Q817 respectively. C816 and C882 reduce the high frequency output impedance of the supplies.

SECTION 6

MAINTENANCE

Introduction

This section of the manual contains maintenance information for use in preventive maintenance, corrective maintenance or troubleshooting of the Type 3S1.

PREVENTIVE MAINTENANCE

General

Preventive maintenance consists of cleaning, visual inspection, lubrication, etc. Preventive maintenance performed on a regular basis will help prevent instrument failure and will improve reliability of this instrument. The severity of the environment to which the Type 3S1 is subjected will determine the frequency of maintenance.

Cleaning

The Type 3S1 should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path.

The top and bottom covers of the 560-series instruments into which the Type 3S1 fits, provide protection against dust in the interior of the instrument. Operating without the covers in place will require more frequent cleaning.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastic used in this instrument. Some chemicals to avoid are benzene, toluene, xylene, acetone or similar solvents.

Exterior. Loose dust accumulated on the outside of the Type 3S1 can be removed with a soft cloth or small paint brush. The paint brush is particularly useful for dislodging dirt on and around the front-panel controls. Dirt which remains can be removed with a soft cloth dampened in a mild solution of water and detergent. Abrasive cleaners should not be used.

Interior. Dust in the interior of the instrument should be removed occasionally due to its electrical conductivity under high-humidity conditions. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air. Remove any dirt which remains with a soft point brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces or for cleaning ceramic terminal strips and circuit boards.

Lubrication

The reliability of potentiometers, rotary switches and other moving parts can be increased if they are kept properly lubricated. Use a cleaning-type lubricant (such as Tektronix Part No. 006-0218-00) on switch contacts. Lubricate switch detents with a heavier grease (such as Tektronix Part No. 006-0219-00). Potentiometers should be lubricated with a lubricant which will not affect electrical characteristics (such as Tektronix Part No. 006-022-00). Do not over-lubricate.

Visual Inspection

The Type 3S1 should be inspected occasionally for such defects as broken connections, improperly seated transistors, damaged circuit boards and heat-damaged parts.

The remedy for most visible defects is obvious; however, care must be take if heat-damaged parts are located. Overheating is usually only a symptom of trouble. For this reason, it is essential to determine the actual cause of overheating before the heat-damaged parts are replaced; otherwise, the damage may be repeated.

Recalibration

To assure accurate measurements, check the calibration of this instrument after each 500 hours of operation or once every six months.

Parts Identification

Identification of Switch Wafers. Wafers of switches shown on the circuit diagram are numbered from the first wafer located behind the detent section of the switch to the last wafer. The letters F and R indicate whether the front or the rear of the wafer is used to perform the particular switching function. For example, the designation 2R printed by a switch section on a schematic identifies the switch section as being on the rear side of the second wafer when counting back from the front panel.

Wiring Color Code. The wiring in the Type 3S1 is color coded to facilitate circuit tracing. In the case of power-supply leads, the color code indicates the voltage carried, with the widest stripe denoting the first significant figure. Table 6-1 lists the color combinations and the voltages indicated by the colors.

All leads that clip to the circuit boards are color coded. The color code of each lead and the pin lettering is shown in parts location figures later on in this section.

Resistor Coding. The Type 3S1 uses a number of very stable metal film resistors identified by their gray background color and color coding.

If the resistor has three significant figures with a multiplier, the resistor will be EIA color coded. If it has four significant figures with a multiplier, the value will be printed on the resistor. For example, a 333 kΩ resistor will be color coded, but a 333.5 kΩ resistor will have its value printed on the resistor body.

The color-coding sequence is shown in Fig. 6-1.

TABLE 6-1
Power Supplies Wire Color Coding

Supply	Color Code
-12.2V	Brown Red Black on Tan
-100V	Brown Black Brown on Tan
+12.2 V	Brown Red Block on White
+100V	Brown Black Brown on White
+125V	Brown Red Brown on White
+300 V	Orange Black Brown on White

Capacitor Marking. The capacitance values of common disc capacitors and small electrolytics are marked in microfarads on the side of the component body. The white ceramic capacitor used in the Type 3S1 are color coded in picofarads using a modified EIA code (see Fig. 6-1).

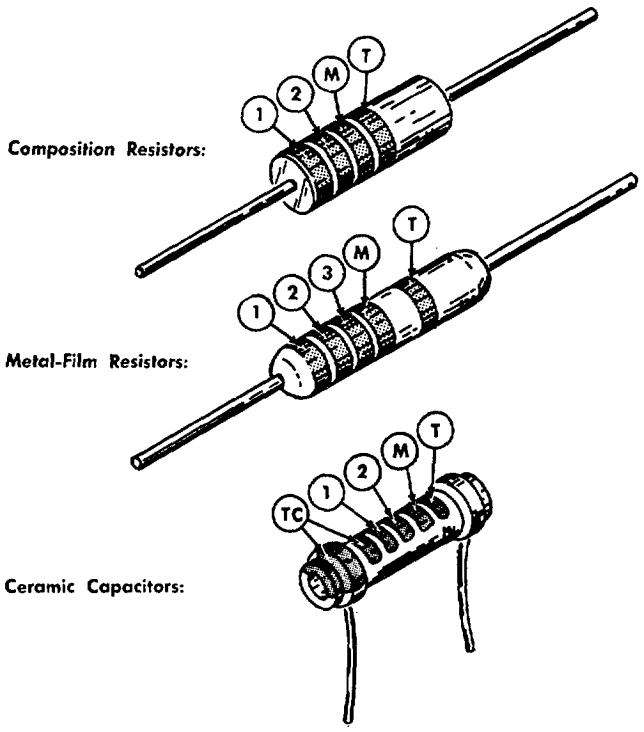
Diode Color Code. The cathode end of each glass-enclosed diode is indicated by a stripe, a dot or a series of stripes. For normal silicon or germanium diodes the stripes also indicate the type of diode, using the resistor color-code system (e.g., 6165 indicates the type of diode with Tektronix Part No. 152-0165-00). The cathode and anode ends of metal-encased diodes can be distinguished by the diode symbol marked on the body or by the flared end of the anode.

Parts Replacement

See page before 9-1 for parts ordering information.

NOTE

When selecting the replacement parts, it is important to remember that the physical size and shape



① ② and ③ -1st, 2nd and 3rd significant figures:

Ⓜ - multiplier; Ⓣ - tolerance;

Ⓣⓒ - temperature coefficient.

Resistor and Capacitor Color Code

Color	Significant Figures	Multiplier		Tolerance	
		Resistors	Capacitors	Resistors	Capacitors
Silver	---	10^{-2}	---	±10%	---
Gold	---	10^{-1}	---	±5%	---
Black	0	1	1	---	±20% or 2 pF*
Brown	1	10	10	± 1%	±1% or 0.1 pF*
Red	2	10^2	10^2	±2%	±2%
Orange	3	10^3	10^3	±3%	3%
Yellow	4	10^4	10^4	±4%	+100% -0%
Green	5	10^5	10^5	±0.5%	±5% or 0.5 pF*
Blue	6	10^6	10^6	---	---
Violet	7	---	---	---	---
Gray	8	---	10^{-2}	---	+80% -20% or 025 pF*
White	9	---	10^{-1}	---	±10% or 1 pF*
(none)	---	---	---	±20%	±10% or 1 pF*

*For capacitance of 10 pF or less.

NOTE: Ⓣ and/or Ⓣⓒ color code for capacitors depends upon manufacturer and capacitor type. May not be present in some cases.

Fig. 6-1. Resistor and ceramic capacitor color code.

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of a component may affect its performance at high frequencies. Parts orientation and lead dress should duplicate those of the original part since many of the components are mounted in a particular way to reduce or control stray capacitance and inductance. After repair, portions of the instrument may require recalibration.

Rotary Switches. Individual wafers or mechanical parts of rotary switches are normally not replaced. If a switch is defective, replace the entire assembly The availability of replacement switches, either wired or unwired, is detailed in the Electrical Parts List.

Circuit Boards. Use ordinary 60/40 solder and a 35- to 40-waft pencil type soldering iron on the circuit boards. The tip of the iron should be clean and properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the etched wiring from the base material.

Most of the components mounted on the A and B Channel circuit boards can be replaced without removing the boards from the instrument. Observe soldering precautions given under Soldering Techniques in this section. However, if the underside of the board must be reached, the delay line and strobe cable must be disconnected from the underside of the board and the mounting screws removed. The interconnecting wires allow the board to be moved out of the way or turned over without removing the square pin connectors from the board. The mounting screws for the A Channel board are shown in Fig. 6-2. The mounting screws for the B Channel board are in the corresponding positions on the right side of the instrument.

The Strobe circuit board is held in place by a single knurled captive screw (Fig. 6-3). Loosening the screw until the threads are disengaged allows the board to be slid up out of the clips holding the end of the board. Connections to the Strobe board are soldered, with the exception of the small coaxial connectors. These connectors may be removed easily, if desired, by pulling straight out.

The preamp input correction circuits on the A and B boards are protected by small metal shields. These shields may be removed by grasping with the fingers and pulling straight out. See Fig. 6-2. The shields are replaced by inserting the shield corner pins in the correct pin-jacks and pressing gently. Be sure the shields are properly oriented; i.e., with the access holes over the adjusting screws in the capacitors.

Components in the Snap-off Circuit located on the Strobe (center) circuit board assembly are isolated by a shield. See Fig. 6-3. This shield may be removed by disconnecting the two coaxial connectors, inserting a small screwdriver under the shield edges, and prying the shield upward gently. When the shield is replaced, the small cutout section should be placed so as to clear the two resistors. In replacing the two coaxial connectors, check that they are not interchanged. The connector towards the front of the instrument should be connected to the A board.

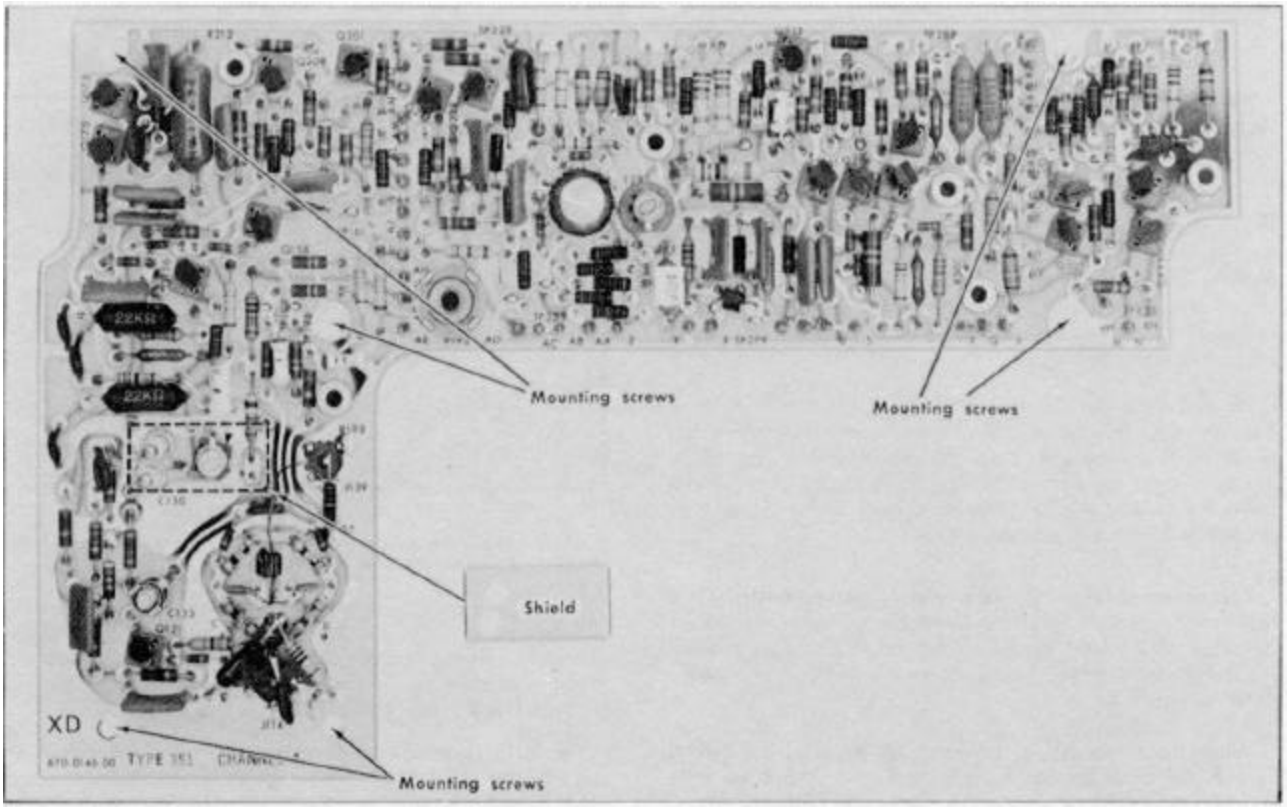

Fig. 6-2. Channel A circuit board with shield removed.

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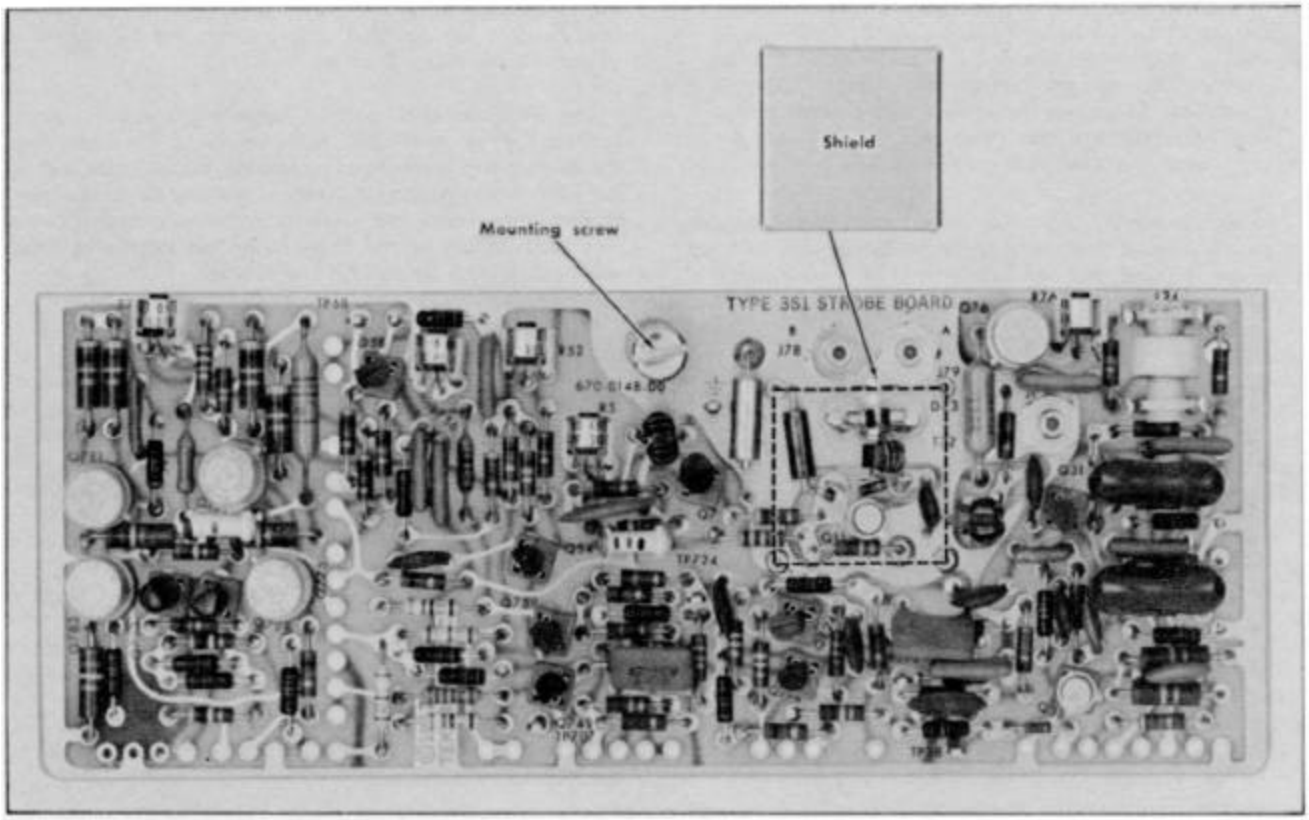

Fig. 6-3. Strobe board with shield removed.

Replacement of soldered-in diodes. Grasp the diode lead between the body of the diode and the circuit board with a small pair of tweezers.

Touch the tip of the soldering iron to the lead where it enters the circuit board. Do not lay the iron tip directly on the circuit board. Gently but firmly pull the diode lead from the hole in the circuit board. If removal of the lead does not leave a clean hole, apply a sharp object such as a toothpick or pointed tool while reheating the solder. Avoid using too much heat.

To place the new diode, bend the leads and trim to fit just through the board. Tin each lead while using the tweezers as a heat sink. Place the diode leads in the holes. Apply a small amount of solder, if necessary, to assure a good bond. Use the tweezers as a heat sink and use only enough heat for a good connection.

Replacement of other soldered-in components. Grip the component lead with long-noise pliers. Touch the soldering iron to the lead at the solder connection. Do not lay the iron directly on the board, as it may damage the board. Refer to Fig. 6-4.

When the solder begins to melt, pull the lead out gently. This should leave a clean hole in the board. If not, the hole can be cleaned by reheating the solder and placing a sharp object such as a toothpick or pointed tool into the hole to clean it out.

Bend the leads of the new component to fit the holes in the board. If the component is replaced while the board is mounted in the instrument, cut the leads so they will just protrude through the board.

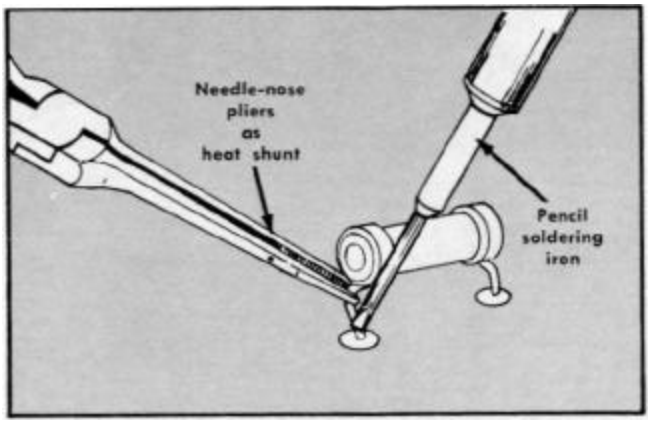

Fig. 6-4. Apply the soldering iron to the heat-shunted lead when removing a component from a circuit card.

Pre-tin the leads of the component by applying the soldering iron and a small amount of solder to each (heat-shunted) lead. Insert the leads into the board until the component is firmly seated against the board. If it does not seat properly, heat the solder and gently press the component into place.

Apply the iron and a small amount of solder to the connection to make a firm solder joint. To protect heat-sensitive components, hold the lead between the component body and the solder joint with a pair of long-noise pliers or other heat sink.

Clip the excess lead that protrudes through the board.

Clean the area around the soldered connection with a flux-remover solvent to maintain good environmental characteristics. Be careful not to remove information printed on the board.

Leadless Capacitors. There are leadless ceramic capacitors soldered directly to the Strobe circuit board. Care must be taken when replacing these capacitors as they are easy to crack. The type of solder used must be high quality, with good cold-flow characteristics. Thus, do not use 50/50 solder, but 60/40 or 62/38 solder when replacing the leadless capacitors.

Best results will be obtained by applying heat from the soldering iron directly under the leadless capacitor on the opposite side of the board. Plated-through holes carry heat through the board to the underside of the capacitor and minimize the chance of cracking the capacitor disk with too much heat.

Use only enough solder to obtain a good full-flow joint. Excess solder on either side of the capacitor can lead to a short circuit.

Metal Terminals. When soldering metal terminals (e.g., switch terminals, potentiometers, etc.), ordinary 60/40 solder can be used. The soldering iron should have a 40- to 75-watt rating with a 1/8 inch wide chisel-shaped tip.

Observe the following precautions when soldering metal terminals:

1. Apply only enough heat to make the solder flow freely.
2. Apply only enough solder to form a solid connection. Excess solder may impair the function of the part.
3. If a wire extends beyond the solder point, clip off the excess.
4. Clean the flux from the solder joint with a flux-remover solvent to maintain good environmental characteristics.

Removal and Replacement of Sampling Diodes. The Sampling Bridge Diodes are mounted in small metal clips, as shown on the circuit board illustrations. The diodes should not be touched with the fingers, and are best removed or replaced with a pair of shaped forceps, such as Tektronix Part No. 006-0765-00, or equivalent. Before inserting the diodes in their clips, it is wise to touch the metal chassis with one hand to discharge any static electricity on the operator's body. Such static electricity discharge occurring through the diode upon first contact with the clip could damage the diode.

Subassembly Removal

Circuit Board Replacement. If a circuit board is damaged and cannot be repaired, the entire assembly including all soldered-on components should be replaced. The part number given in the Mechanical Parts List is for the completely wired board.

Procedure for replacing circuit boards follows:

For the A and B Channel circuit boards,

1. Disconnect all square pin and coaxial connectors by pulling straight out from the board.
2. Remove the board mounting screws (Fig. 6-2).
3. Install the replacement board and replace the mounting screws.
4. Replace the square pin and coaxial connectors, referring to the wire color coding and pin identification information at end of this section.

For the Strobe circuit board,

1. Loosen the single knurled captive screw (Fig. 6-3).
2. Slide the board up out of the mounting clips.
3. Disconnect the coaxial connectors by pulling straight out from the board.
4. Carefully unsolder the wires from the board, using the precautions given under Soldering Techniques in this section.
5. Solder the wires to the replacement board, using the minimum amount of heat and solder as suggested previously under Soldering Techniques. Refer to the wire color coding information for the Strobe circuit board at the end of this section.
6. Connect the coaxial connectors, and slide the board into the clips, taking care that the coaxial cables do not dislodge transistors while sliding the board into place.

TROUBLESHOOTING

Introduction

The following information is provided to facilitate troubleshooting of the Type 3S1 if trouble develops. Information contained in other sections of this manual should be used along with the following information to aid in locating the defective component.

Troubleshooting Aids

Diagram. Circuit diagrams are given on foldout pages in Section 11. The circuit number and electrical value of each component in this instrument are shown on the diagram. Important voltages and waveforms are also shown on the diagrams.

Component Numbering. The circuit number of each electrical port is shown on the circuit diagram. Each main circuit is assigned a series of circuit numbers. Table 6-2 lists the main circuit in the Type 3S1 and the series of circuit numbers assigned to each. For example, using Table 6-2, a resistor numbered R615 is identified as being located in the Channel B Amplifier.

TABLE 6-2

Circuit Numbers on Schematics	Circuit
1-100	Gate Generators
100-199	Channel A Sampler
200-299	Channel A Memory
300-399	Channel A Amplifier
400-499	Channel B Sampler
500-599	Channel B Memory
600-699	Channel B Amplifier
700-799	Output Amplifier
800-889	Power Supply and Distribution
890-899	Digital Logic

Troubleshooting Techniques

This troubleshooting procedure is arranged in an order which checks the simple trouble possibilities before proceeding with extensive troubleshooting. The first few checks assure proper connection, operation and calibration. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located, it should be replaced following the replacement procedures given in this section.

1. Check Associated Equipment. Before proceeding with troubleshooting of the Type 3S1 check that the equipment used with the Type 3S1 is operating correctly. Check that the signal is properly connected and that the interconnecting cables are not defective. Also, check the power source.

2. Check Control Settings. Incorrect control settings can indicate a trouble that does not exist. For example, incorrect setting of the Vertical Units/Div VARIABLE control appears as incorrect gain, etc. If there is any question about the correct function or operation of any control, see the Operating Instructions section of this manual.

3. Check Instrument Calibration. Check the calibration of the instrument, or the affected circuit if the trouble exists in one circuit. The indicated trouble may only be a result of misadjustment or may be corrected by calibration. Complete instructions are given in the Calibration section of this manual.

4. Isolate the Trouble to a Circuit. If the trouble has not been corrected or isolated to a particular circuit with the preceding steps, make the following checks if possible.

a. Check for the correct resistance readings at the interconnecting plug terminals, as indicated in Table 6-3.

If the resistance values at the interconnecting plug are equal or higher than stated in Table 6-3, proceed with the next step.

TABLE 6-3
Interconnecting Plug Resistance Checks
Type 3S1 disconnected from Oscilloscope
(pin numbers omitted are unconnected)

Pin Number	Resistance to Ground	With Ohmmeter Leads Reversed
1	infinite	infinite
2	infinite	infinite
3	0	0
4	370 Ω	370 Ω
9	0	0
10	11.5 kΩ	41 kΩ
11	24 kΩ	21 kΩ
12	54 kΩ	52 kΩ
15	4 kΩ	4.2 kΩ
16	370 Ω	660 Ω
17	12 kΩ	42 kΩ
18	0.2 Ω	0.2 Ω
19	0	0
20	8.6 kΩ	8.4 kΩ
21	13.5 kΩ	35 kΩ
22	4 kΩ	4 kΩ
23	4.2 kΩ	5.1 kΩ
24	10 kΩ	5.6 kΩ

b. Connect the Type 3S1 to the oscilloscope in which it will normally operate. Use the flexible cable extension, Tektronix Part No. 012-0066-00. Turn on the instrument and allow at least 5 minutes warm-up time.

Check the power supply voltages. Convenient test points are shown in Table 6-4 and Fig. 6-5, 6-6 and 6-7.

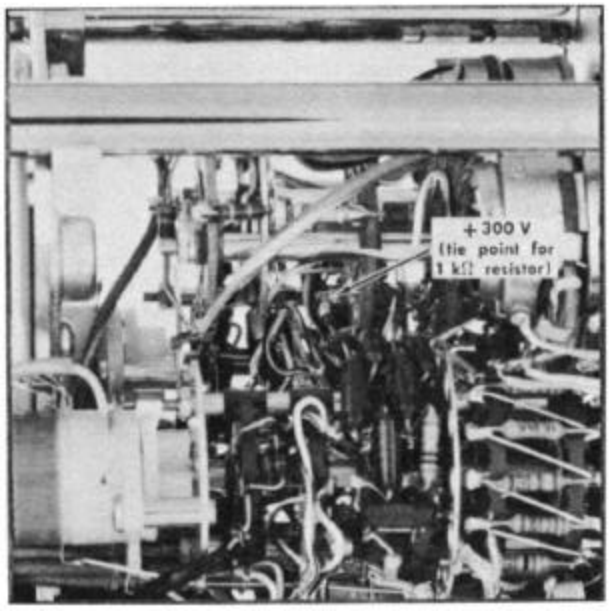

Fig. 6-5. Location of test point for +300 volt supply (left side of Type 3S1, DUAL-TRACE switch wafer 3R).

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Incorrect operation of all circuits often indicates trouble in the power supplies. Check first for correct adjustment of the individual supplies. However, a defective component elsewhere in the instrument can appear as a power-supply trouble and may also affect the operation of other circuits.

Table 6-4 shows the tolerance of the two internal power supply voltages, and the normal voltages supplied by the oscilloscope. If a power supply voltage is within the listed tolerances, the supply can be assumed to be working correctly. If outside the tolerances, the +12.2 volt adjustment may be incorrect, or component in the non-adjustable +100 volt supply may be defective.

TABLE 6-4

Power Supply	Tolerance	Test Point Number and Location
+12.2 V[1]	±0.12V	TP839 A Board
+100 V	±5 V	TP817 A Board
+125 V	±3.8 V	Pin AH, B Board
+300 V	±9 V	See Fig. 6-5
-12.2 V	±0.37 V	Pin S, B Board
-100 V	±3 V	Pin V, B Board

[1]Adjusted by R832.

Power Supply voltage checks may be made at the points indicated in Table 6-4 and Fig. 6-5, 6-6 and 6-7.

Table 6-5 shows typical voltage readings at the various test points, with the front-paned controls set as follows:

A and B DC OFFSET controls	Adjusted for 0 volts at OFFSET OUT jacks
A and B POSITION controls	Centered
Mode Switch	Channel A
INTERNAL TRIGGER	A
A and B mVOLTS/DIV	200
SMOOTH / NORMAL	NORMAL

CAUTION

When making checks with the Strobe board pulled up out of the retaining clips and the instrument turned ON, do not allow the underside of the board to touch the plug-in chassis at any point. Severe damage to components may result. In addition, the cases of transistors Q771, Q781, Q775 and Q785 are elevated to +300 volts above ground, and should not be touched while the instrument is turned on.

NOTE

Voltages and waveforms given on the diagrams are not absolute and may vary slightly between instruments. To obtain operating conditions similar to those used to take these readings, see the first schematic page.

Transistor Checks

Transistors should not be replaced unless they are actually defective. Transistor defects usually take the form of the transistor opening, shorting or developing excessive leakage. To check a transistor for these and other defects, use a transistor curve display instrument such as a Tektronix Type 575. However, if a good transistor checker is not readily available, a defective transistor can be found by signal-tracing, by making in-circuit voltage checks, by measuring the transistor forward-to-back resistance using proper ohmmeter resistance ranges, or by using the substitution method. The location of all transistors is shown in the parts location figures later in this section.

To check transistors using a voltmeter, measure the emitter-to-base and emitter-to-collector voltages and determine if the voltages are constant with the normal resistances and currents in the circuit (see Fig. 6-9).

To check a transistor using an ohmmeter, know your ohmmeter ranges, the currents they deliver and the internal battery voltage(s). If your ohmmeter does not have sufficient

TABLE 6-5
Test Point Voltage Readings

A Circuit Board Test Point	Voltage Reading	B Circuit Board Test Point	Voltage Reading	Strobe Board Test Point	Voltage Reading
161	0	461	0	38	-36
196	+1.22	496	+1.6	58	-10.5[2]
199	-1.22	499	-1.4	707	-0.92
229	+7.1	529	+7.3	714	-0.54
235	-12[2]	535	-12[2]	724	+ 10.5
279	-0.22	579	-0.14		
288	+0.3	588	+0.16		
313	+9.5	613	+10		
838	+20	817	+100		
839	+12.2[3]				

[2]Value based on series decoupling resistor. See Power Distribution and Connector schematic.
[3]Adjusted by R832.

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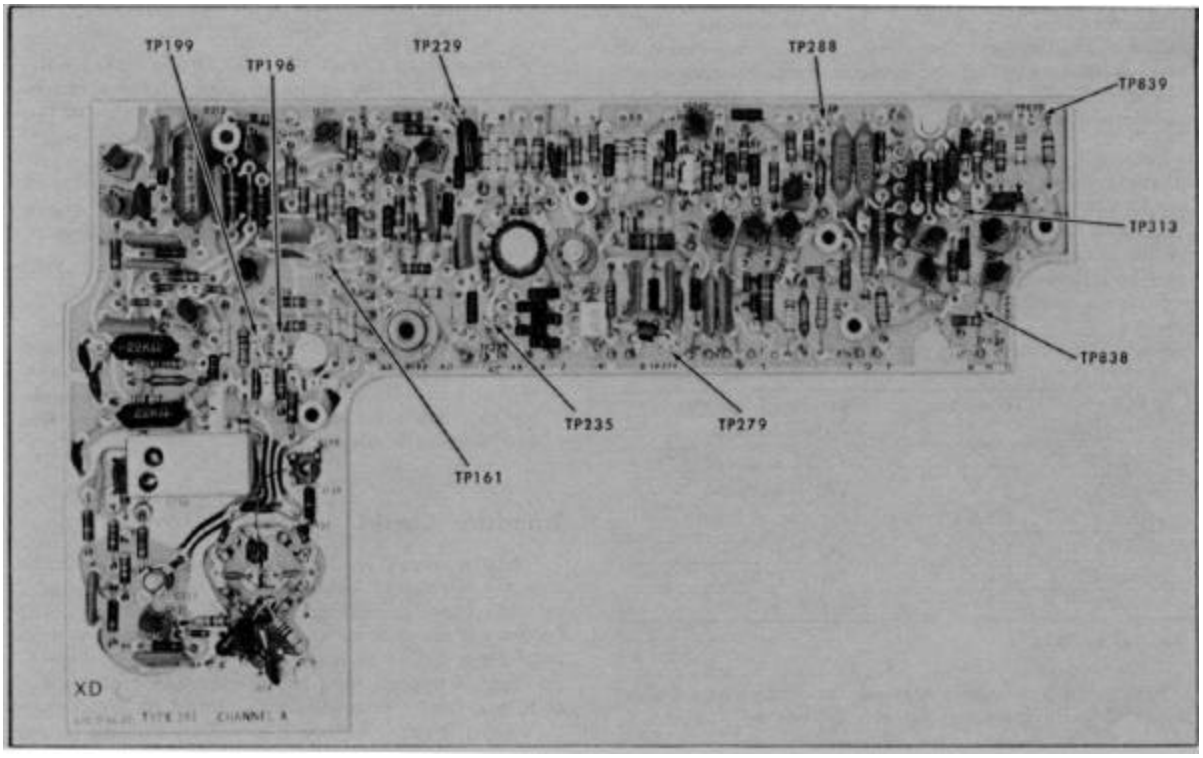

Fig. 6-6. Test point locations, A circuit board.

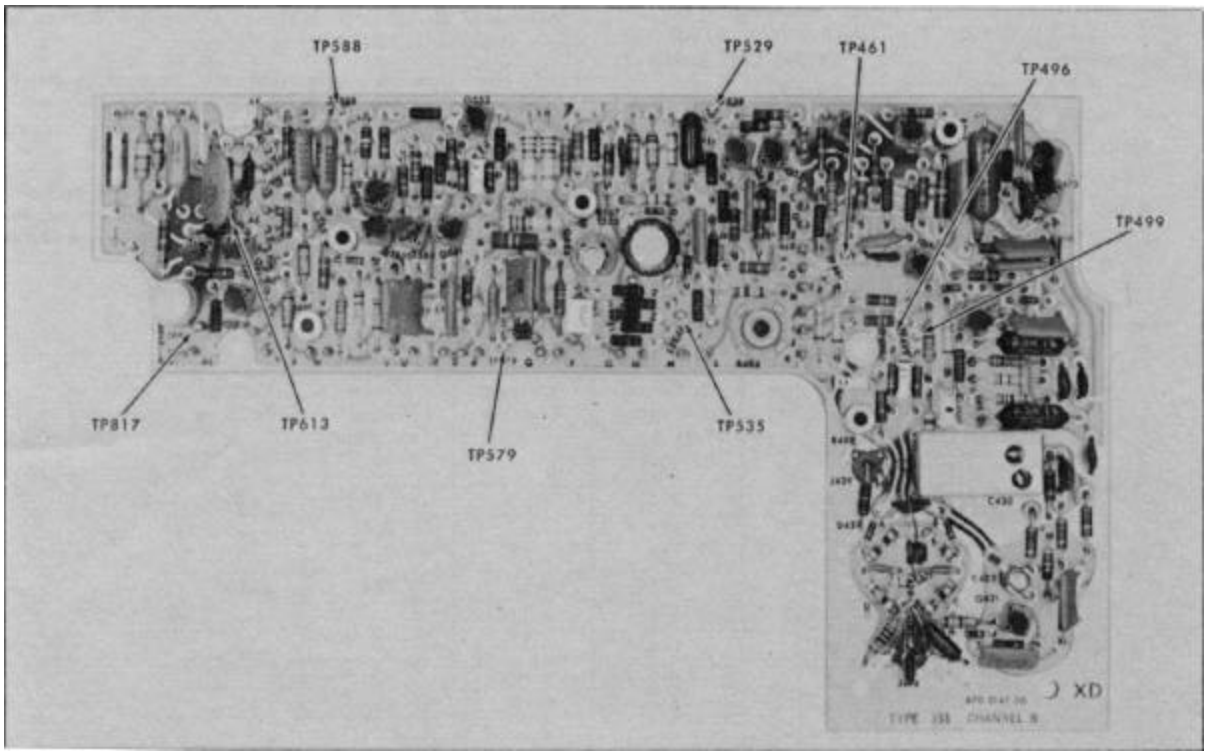

Fig. 6-7. Test point locations, B circuit board.

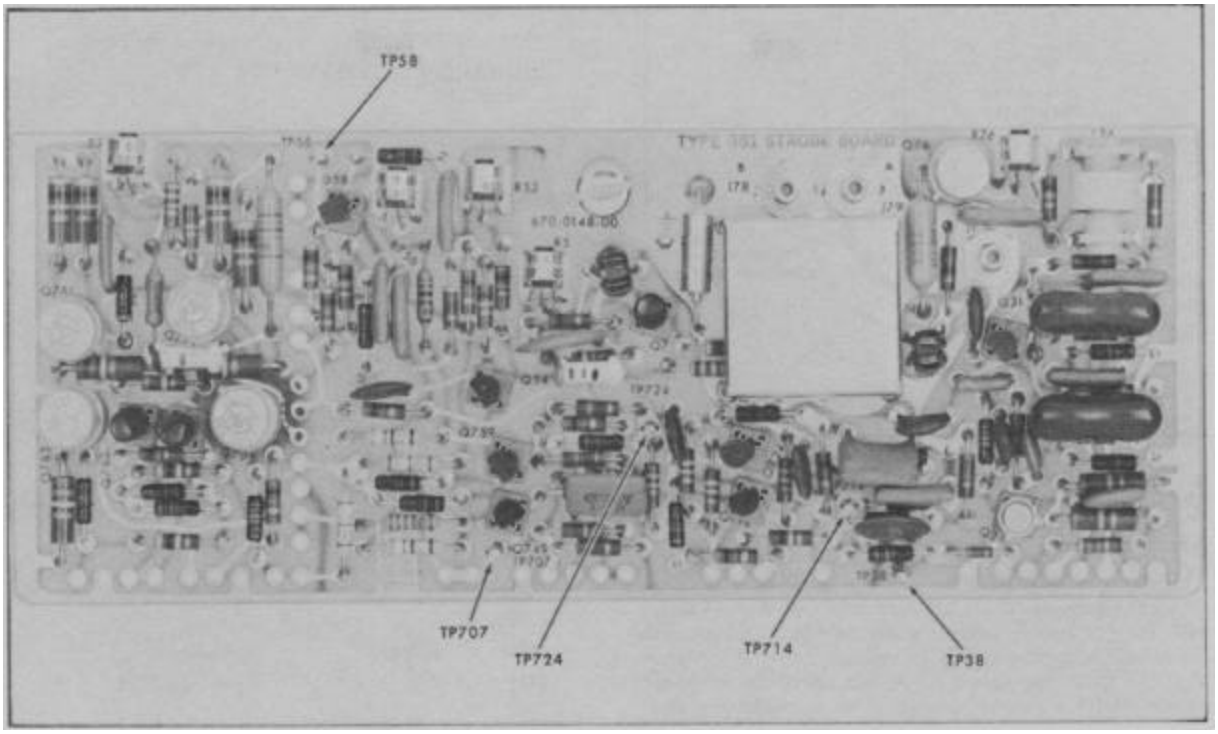

Fig. 6-8. Test point locations, Strobe circuit board.

resistance in series with its internal voltage source, excessive current will flow through the transistor under test. Excessive current and/or high internal source voltage may permanently damage the transistor.

NOTE

As a general rule, use the R X 1 K range where the current is usually limited to less than 2 mA and the internal voltage is usually 1 1/2 volts. You can quickly check the current and voltage by inserting a multimeter between the ohmmeter leads and measuring the current and voltage for the range you intend to use.

When you know which ohmmeter ranges will not harm the transistor, use those ranges to measure the resistance with the ohmmeter connected both ways as given in Table 6-6.

If there is doubt about whether the transistor is good, substitute a new transistor; but first be certain the circuit voltage applied to the transistor are correct before making the substitution.

When checking transistors by substitution, be sure that the voltages on the transistor are normal before making the substitution. If a transistor is substituted without first checking out the circuit the new transistor may immediately be damaged by some defect in the circuit.

TABLE 6-6
Transistor Resistance Checks

Ohmmeter Connections [4]	Resistance Readings That Can Be Expected Using the R X 1 k Range
Emitter-Collector	High readings both ways (about 60 kΩ to around 500 kΩ).
Emitter-Base	High reading one way (about 200 kΩ or more). Low reading the other way (about 400 Ω to 2.5 kΩ).
Base-Collector	High reading one way (about 500 kΩ or more). Low reading the other way (about 400 Ω to 2.5 kΩ).

[1]Test prods from the ohmmeter are first connected one way to the transistor leads and then the test prods are reversed (connected the other way). Thus, the effects of the polarity reversal of the voltage applied from the ohmmeter to the transistor can be observed.

CAUTION

Be careful when making measurements on live circuits. The small size and high density of components used in this instrument result in close spacing. An inadvertent movement of the test probes, or the use of oversized probes may short between circuits.

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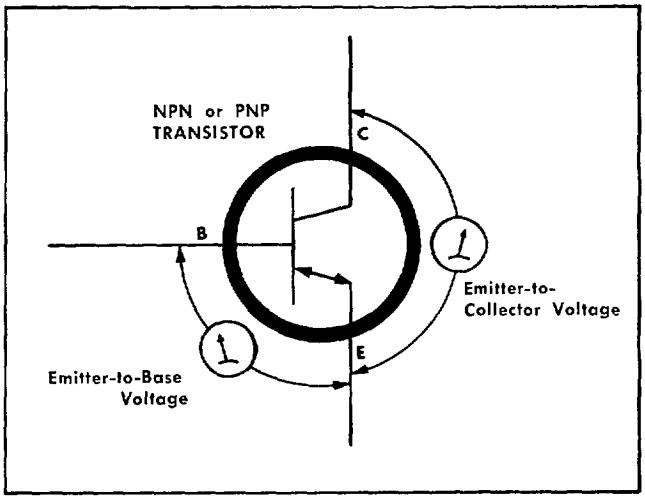

Fig. 6-9. In-circuit voltage checks NPN or PNP transistors.

Diode Checks

A diode can be checked for an open or shorted condition by measuring the resistance between terminals. With an ohmmeter scale having an internal source of about 1.5 volts, the resistance should be very high in one direction and very low when the leads are reversed. Do not check the sampling diodes with an ohmmeter. Change sampling diodes any time you cannot properly adjust the Blow-by compensation; see step 33 of the Calibration Procedure.

CAUTION

Do not use an ohmmeter scale that has a high internal current. High currents may damage the diode. Do not measure tunnel diodes with an ohmmeter; use a dynamic tester (such as Tektronix Type 575 Transistor-Curve Tracer).

Field Effect Transistors (FET)

Field effect transistors in the Type 3S1 should not be tested with an ohmmeter. Rather, if you suspect a dual FET (Q243A or Q243B, both in the some enclosure on the Channel A circuit board or Q543 on the Channel B circuit board), pull the unit out of the socket, rotate it 180° and re-insert it. The leads are arranged in a manner to permit the unit to be installed with the guide pin either straight up or straight down. If there is no change in circuit operation, both sections of the dual FET are probably good. Q243 and Q543 should be replaced if during a calibration procedure, the related Smoothing Balance control cannot be properly adjusted.

Actual condition of either half of an FET can be checked using a Tektronix Type 575 Transistor Curve Tracer. Follow the lead identification of Fig. 6-10 when making connections at the curve tracer sockets.

Set the curve tracer controls:

COLLECTOR SWEEP Controls	
PEAK VOLTS RANGE	20.0
POLARITY	+ [NPN)
PEAK VOLTS Control	Fully counterclockwise
DISSIPATION LIMITING RESISTOR	2K
VERTICAL Controls	
CURRENT OR VOLTAGE	1 COLLECTOR MA
POSITION	Spot at lower left corner of graticule
HORIZONTAL Controls	
VOLTS/DIV	10 COLLECTOR VOLTS
POSITION	Spot at lower left corner of graticule
BASE STEP GENERATOR Controls	
REPETITIVE/OFF/SINGLE FAMILY	REPETITIVE
STEPS/FAMILY	Fully counterclockwise
POLARITY	---
STEPS/SEC	120 (up)
SERIES RESISTOR	Optional
STEP SELECTOR	.2 MA PER STEP
Slope Panel Controls	
Center rotary switch	EMITTER GROUNDED

Connect a 1000Ω (1% or 5%) 1/2 watt resistor between the B and E binding posts on whichever side of the sloping panel you plan to test the FET. This resistor develops a voltage bias

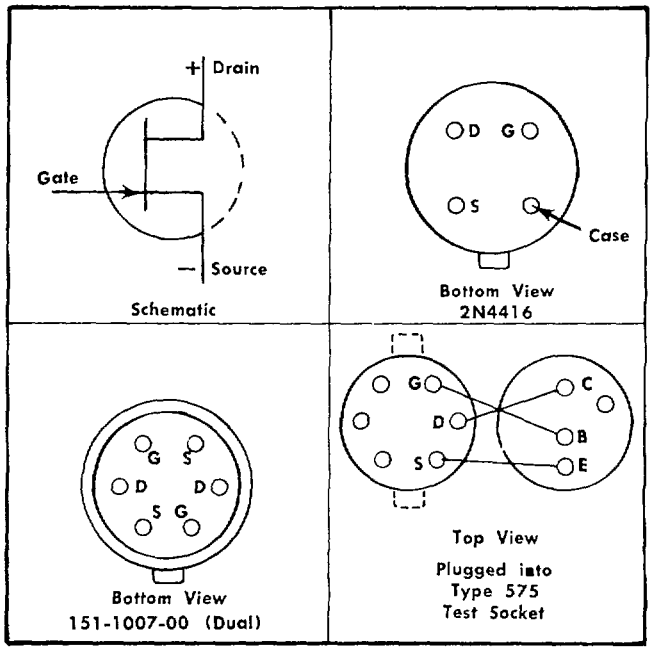

Fig. 6-10. Pin arrangements on FET's used in Type 3S1.

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for the Gate lead at 1 volt per mA base step current.

Since the leads of the FET are short, you can avoid bending them (with a chance of breakage) by building an adapter out of a spare transistor socket and wire leads to the sloping panel binding posts. Follow Fig. 6-10 when making connections.

151-1007-00

Zero-bias channel current (Idss) is a minimum of 1.5 mA at 10 volts. Minimum Gm is 1000 *m*mhos at a drain current of 1 mA.

2N4416

Drain saturation current (Idss) is 5 mA to 15 mA with drain-source voltage at 15 volts. Minimum Gm is 4500 *m*mhos at zero gate-source voltage and drain-source voltage at 15 volts.

Major Circuit and Parts Locations

The remainder of this section includes photographs of sections of the Type 3S1. Major circuit areas are identified. All components mounted on circuit boards are identified by circuit numbers. All circuit board connections are identified by pin number or color code.

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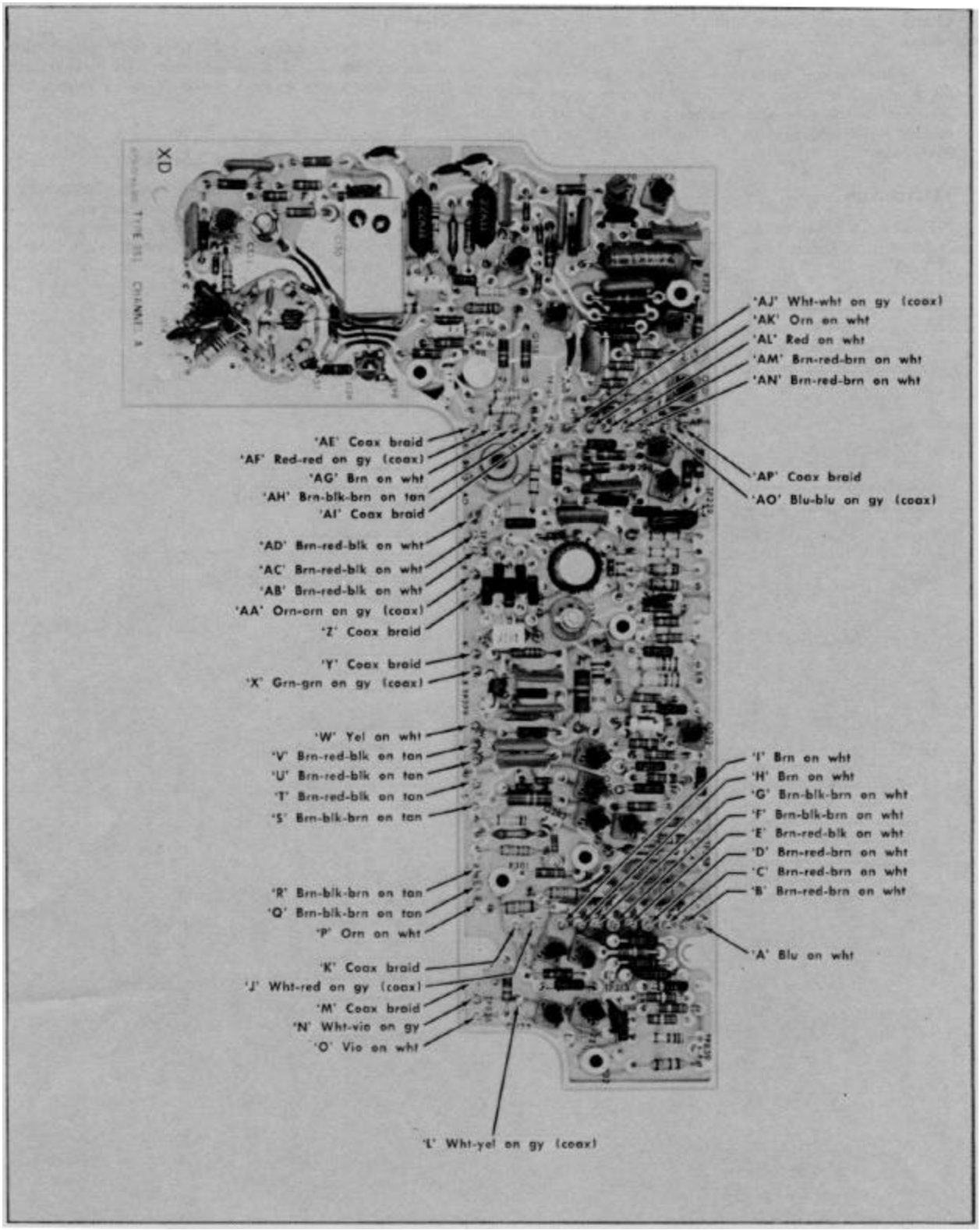

Fig. 6-11. Channel A circuit board assembly wiring color code.

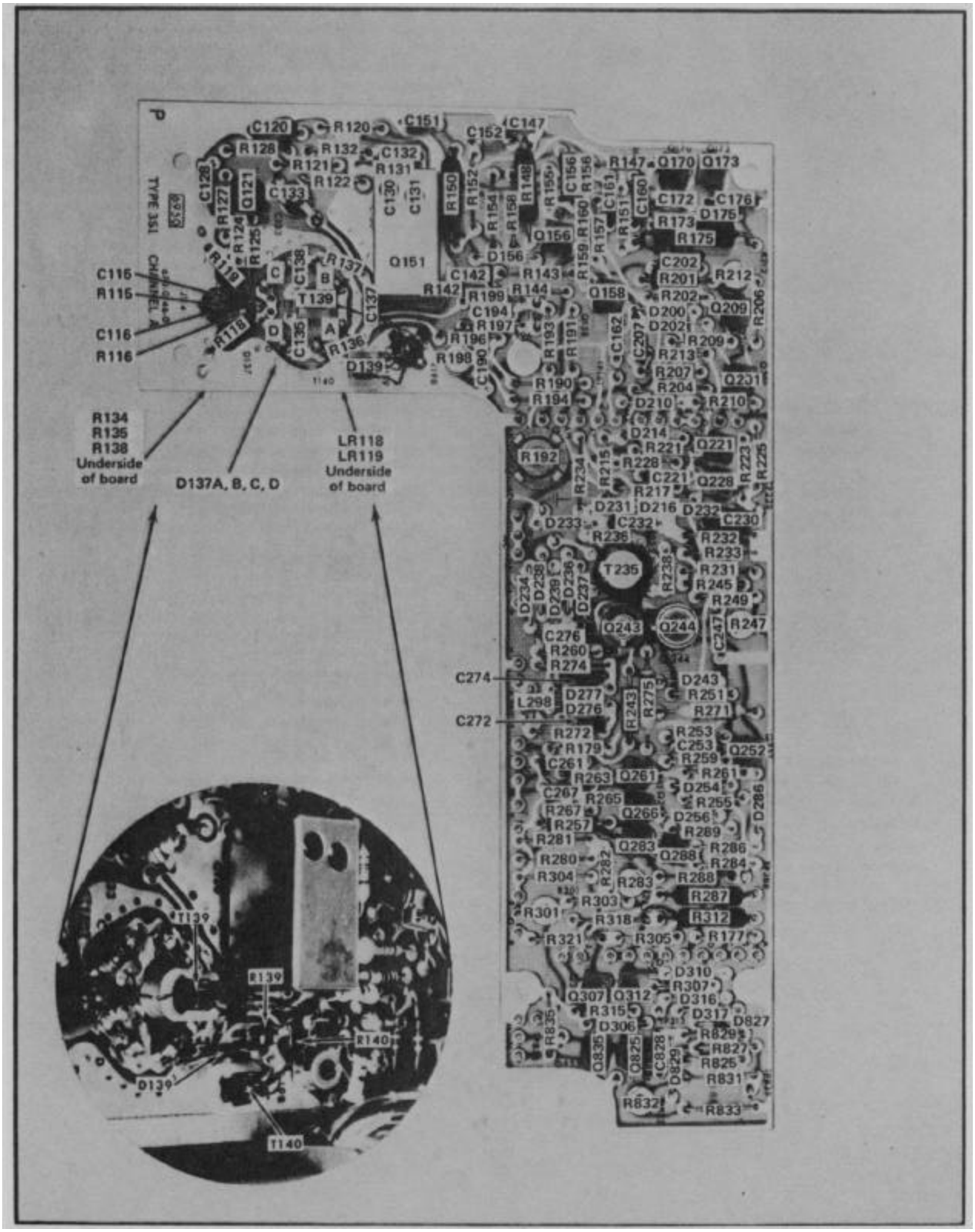

Fig. 6-12. Channel A circuit board assembly parts location.

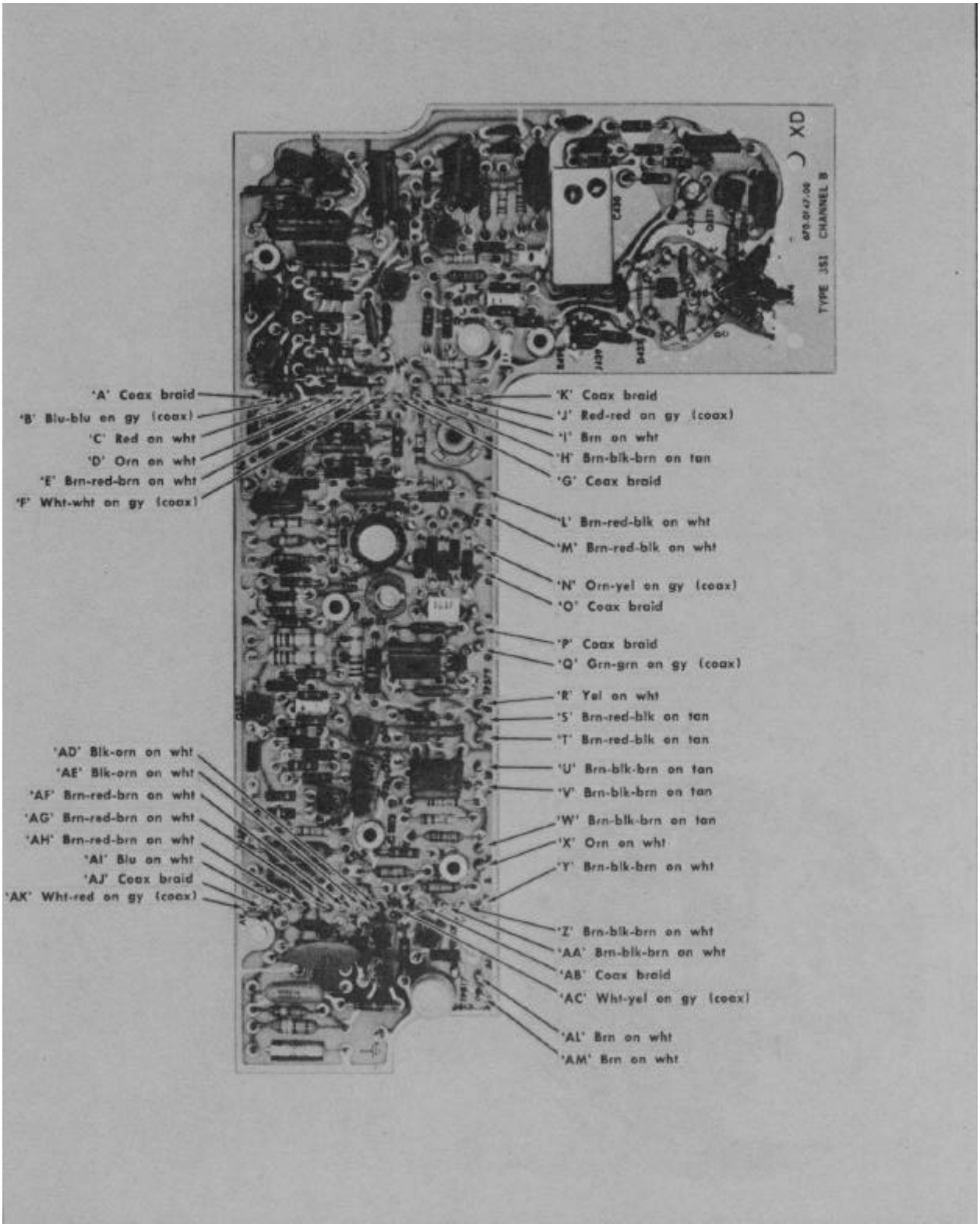

Fig. 6-13. Channel B circuit board assembly wiring color code.

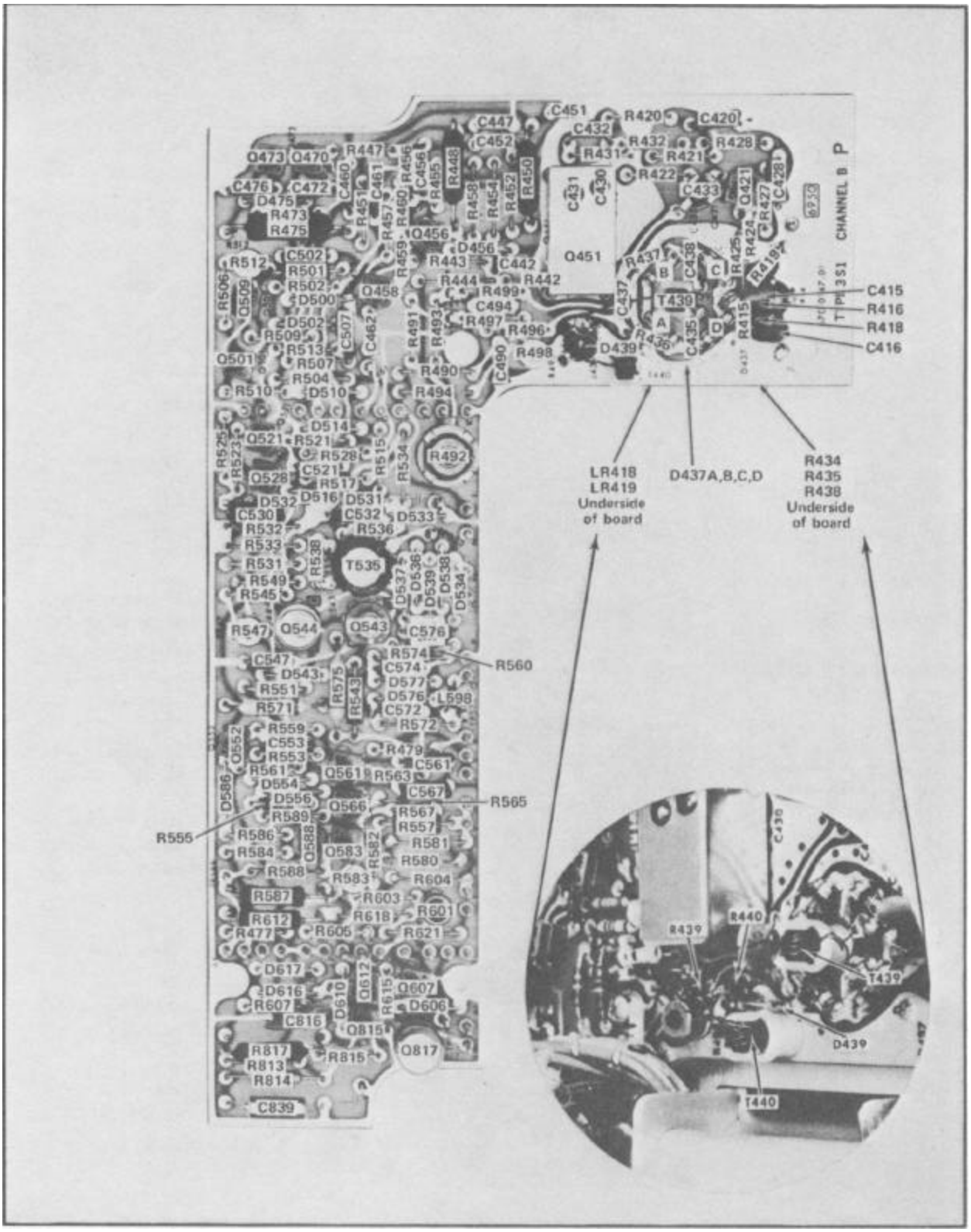

Fig. 6-14. Channel B circuit board assembly parts location.

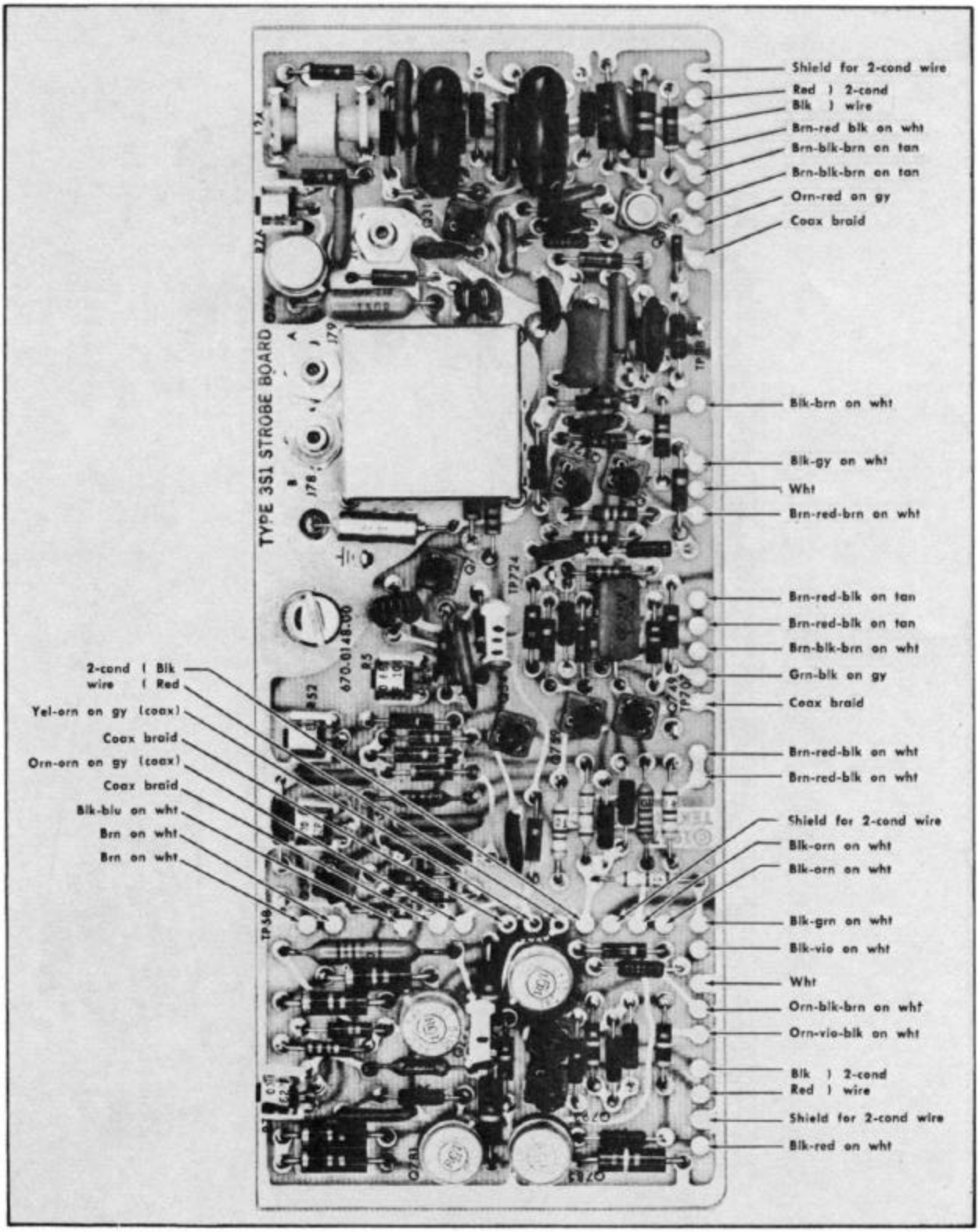

Fig. 6-15. Strobe circuit board assembly wiring color code.

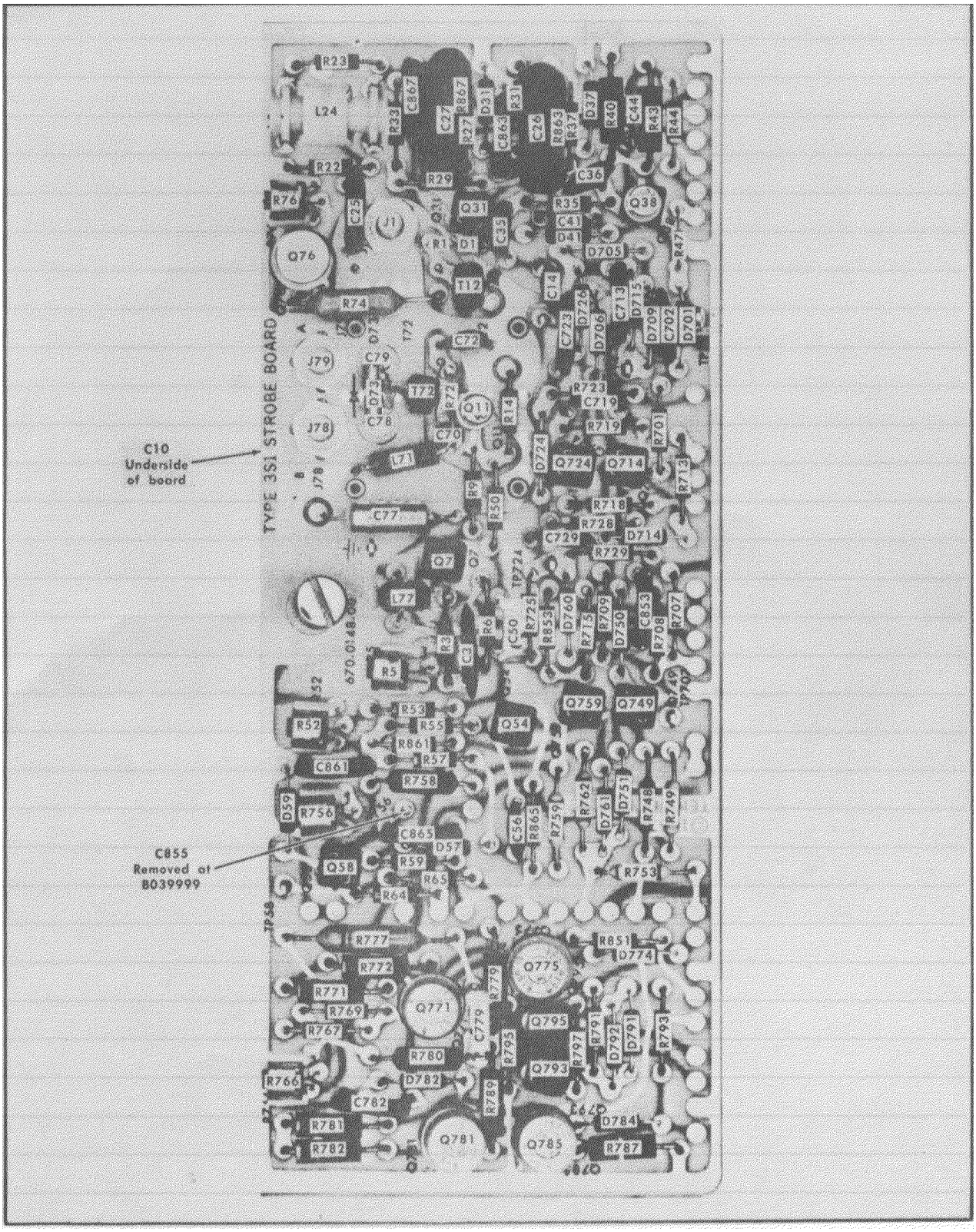

Fig. 6-16. Strobe circuit board assembly parts location.

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NOTES

SECTION 7
PERFORMANCE CHECK

Introduction

This section of the manual provides a means of rapidly checking the performance of the Type 3S1. It is intended to check the calibration of the instrument without the need for performing the complete Calibration Procedure. The Performance Check does not provide for the adjustment of any internal controls. Failure to meet the requirements given in this procedure indicates the need for internal checks or adjustments, and the user should refer to the Calibration Procedure in this manual.

Suggested Equipment

The following equipment is suggested for a complete performance check. Specifications given are the minimum necessary to perform this procedure. All equipment is assumed to be calibrated and operating within the original specifications. If equipment is substituted, it must meet or exceed the specifications of the suggested equipment.

For the most accurate and convenient performance check, special calibration fixtures are used in this procedure. These calibration fixtures are available from Tektronix, Inc. Order by part number through your local Tektronix Field Office or representative.

1. Oscilloscope. Bandwidth DC to 20 MHz; minimum deflection, 20 mV/div; DC comparison voltage for accurate DC voltage measurements; Tektronix Type 545B with a W Plug-In Unit is suggested.

2. Oscilloscope, Tektronix Type 561A equipped with a Sampling Sweep unit for use with the Type 3S1. (Type 3T77A Sampling Sweep unit is used in the Performance Check).

3. 50Ω Amplitude Calibrator. Output impedance 50 Ω; voltage range, .012 to 2.0 volts square wave; accuracy, within ±0.25%. For example, Tektronix Part No. 067-0508-00.

4. Fast Rise Pulse Generator. Risetime requirement, ≤80 ps. Output impedance, 50 Ω; Tektronix Calibration Fixture 067-0513-00 is suggested (risetime ≤30 ps).

5. Square-Wave Generator. Risetime, less than 20 ns; amplitude 600 millivolts; impedance, 50 Ω. Tektronix Type 106 Square-Wave Generator is suggested.

6. Pulse Generator. Risetime of negative-going edge, ≤0.75 ns; pulse amplitude, approximately 460 mV; pulse width, ≥5 ms; flatness, ≤2% overshoot and ringing following negative-going edge of pulse; ≤0.5% aberration 10 ns after negative-going edge of pulse. Tektronix Type 281 Time-Domain Reflectometer Pulser is required.

7. Two 10X attenuators. Impedance, 50 Ω; GR 874-G20; Tektronix Part No. 017-0078-00.

8. One 5X attenuator. Impedance, 50 Ω; BNC connectors; Tektronix Part No. 011-0060-00.

9. Two coaxial cables. BNC connectors; impedance 50 Ω; Tektronix Part No. 012-0057-01.

10. 20 or 30 cm air line. Impedance 50 Ω; Tektronix Part No. 017-0084-00 (for 20 cm air line).

11. Tee connector. Impedance 50 Ω; GR 874-T; Tektronix Part No. 017-0069-00.

12. Two 50 Ω connecting cables, 5 ns delay, with GR Type connectors. Tektronix Part No. 017-0502-00.

13. Termination. Impedance 50 Ω, GR 874-W50B. Tektronix Part No. 017-0081-00.

14. Probe. 1X attenuation for use with the Type W. Tektronix Part No. 010-0074-00.

15. Resistance Bridge, accurate within ±0.2% or better at 50 Ω. ESI Model PVB 300 or equivalent.

16. Tektronix Type 3B2 Analog/Digital time base unit is used in real time checks if required. (Optional check step 20).

17. Tektronix Type 2B67 time base unit is used for real time checks. (Optional check step 21).

18. Tektronix Type 567 with Type 6R1A is used if digital operational checks are required. (Optional check steps 18, 19 and 20).

PERFORMANCE CHECK PROCEDURE

General

In the following procedure, test equipment connections or control settings should not be changed except as noted. If only a partial check is desired, refer to the preceding step(s) for setup information.

The following procedure uses the equipment listed under Suggested Equipment. If substitute equipment is used, control setting or setup must be altered to meet the requirements of the equipment used.

Preliminary Procedure

a. Turn the Power switch of the Type 561A to off position until after step 1 is completed. Plug the Type 3S1 into the left compartment in the Type 561A Oscilloscope. Plug the Type 3T77A sampling sweep unit into the right compartment

b. Set controls as follows:

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Type 3S1

Display Mode switch	CHAN A
SMOOTH-NORMAL switch	NORMAL
A POSITION	Midrange
B POSITION	Midrange
DC OFFSET ±1 V, Channel A	Midrange (5 turns from one end)
DC OFFSET ±1 V, Channel B	Midrange (5 turns from one end)
mVOLTS/DIV, Channel A	200
mVOLTS/DIV, Channel B	200
VARIABLE mVolts/Div (both channels)	CAL
INVERT-NORM switch, Channel A	NORM
INVERT-NORM switch, Channel B	NORM
INTERNAL TRIGGER	OFF
HORIZ PLUG-IN	SAMPLING 3T-SERIES

Type 3T77A

Horizontal Position	Midrange
Time/div	2 ms/div
Time Expander	X 1
Time Position	Clockwise
Dots Per div	100
Trigger Sensitivity	Clockwise
Trigger	Ext +
Sweep Mode	Normal

1. Check Input Resistance

Requirement - The DC resistance of the input must be 50 Ω, ±1 Ω.

a. Connect an accurate ±0.2% resistance bridge between the center and outer conductors of the A INPUT connector.

b. Measure the resistance between the inner and outer conductors of the coaxial connector with the INTERNAL TRIGGER switch set to OFF.

c. Remove the test leads and short them together. Measure the lead resistance.

d. Subtract the value of the lead resistance from the overall resistance for a net resistance value of 50 Ω ±1 Ω.

e. Set the INTERNAL TRIGGER switch to A and repeat the measurement.

f. Repeat the measurement procedure for B INPUT, using the INTERNAL TRIGGER switch first in the OFF position and then in the B position. All measurements must be 50 Ω ±1 Ω. Reset the INTERNAL TRIGGER switch to OFF.

g. Remove the test leads. Turn the Type 561A Power switch on and allow a 20-minute warm up before proceeding.

2. Check mVOLTS/DIV Accuracy

Requirement - Accuracy within ±3% of that indicated on the mVOLTS/DIV switch with the INVERT-NORM switch in the NORM position. Accuracy within ±5% of that indicated on the mVOLTS/DIV switch with the INVERT-NORM switch in the INVERT position.

a. Connect the signal output from the 50 Ω Amplitude Calibrator through a 5 ns coaxial cable to the A INPUT connector of the Type 3S1.

b. Connect the Trigger output signal of the 50 Ω Amplitude Calibrator through a 50 Ω coaxial cable and a 5X attenuator to the trigger Ext Input of the Type 3T77A sampling sweep unit

c. Turn the 50 Ω Amplitude Calibrator power on and set the Volts switch to 1.2. Turn the Test-operate switch to the Operate position.

d. Adjust the Trigger Sensitivity on the Type 3T77A for a stable display.

e. Adjust the A POSITION control and the VERT GAIN screwdriver adjustment control on the Type 3S1 to obtain a centered 6 division display.

f. Check the Channel A deflection accuracy for all positions of the A mVOLTS/DIV switch, by setting the 50 Ω Amplitude Calibrator according to Table 7-1.

TABLE 7-1

50 Ω Amplitude Calibrator Setting	Type 3S1 mVOLTS/DIV Switch Setting	Vertical Display Size with INVERT-NORM switch positions	
		NORM ±3%	INVERT ±5%
1.2	200		
.6	100		
.3	50		
.12	20	5.82 to 6.18 div	5.7 to 6.3 div
.06	10		
.03	5		
.012	2		

g. Move the 50 Ω signal cable to the B INPUT connector. Set the Display Mode switch to CHAN B, and repeat the procedure checking the Channel B deflection accuracy.

h. Reset the INVERT-NORM switches to their NORM positions.

3. Check mVolts/Div VARIABLE controls

REQUIREMENT - Each Channel mVolts/Div VARIABLE control will alter each calibrated deflection factor over a range of ≤0.7:1 to ≥2.5:1.

a. Set the Channel B mVOLTS/DIV switch to 200, and the Amplitude Calibrator Volts switch to .6.

b. The Channel B display amplitude should be 3 divisions P-P (peak to peak) when the VARIABLE control is at CAL (detent) position.

c. Turn the VARIABLE control fully counterclockwise. The display should be ≤2.1 divisions P-P.

d. Turn the VARIABLE control fully clockwise. The display should be ≥7.5 divisions P-P.

e. Move the signal cable to the A INPUT connector. Set the Display Mode switch to CHAN A. Repeat the above procedure for Channel A VARIABLE control.

f. Check that the UNCAL lights are on. Return both VARIABLE controls to their CAL position and check that their lights are out.

4. Check A OUT, B OUT Voltage

REQUIREMENT - Output of each channel, A OUT, B OUT, is 200 mVolts per displayed division ±3% with an output impedance of 10 kΩ.

a. Set the 50 Ω Amplitude Calibrator Volts switch to 1.2.

b. Set the test oscilloscope controls as follows:

Type 545B

Horizontal Display	A
Horizontal Position	Midrange
Triggering Mode	AC
Trigger Slope	Int +
Triggering Level	Midrange
Stability	Preset
Time/cm	5 ms
Variable	Calibrated

Type W Plug-In

Display	A-Vc
Input Atten	R ≈ ∞
Millivolts/cm	20
Variable	Cal
Comparison Voltage	0.00
Vc Range	-11
A Input selector	DC
Position	Midrange

c. Connect the signal from the Type 3S1 B OUT jack through a 1X probe to the Type W Input A.

d. Adjust the Position control of the Type W so the positive portion of the square wave (top of the display is at the center of the graticule. Some adjustment of the A Channel DC OFFSET control of the Type 3S1 may be necessary.

e. Set the Comparison Voltage of the Type W so the negative portion of the square wave (bottom of the display) is at the center of the graticule.

f. Read the Comparison Voltage of 1.2 volts ±3%.

g. Move the signal to B INPUT, and move the 1X test probe to the B OUT jack of the Type 3S1. Repeat the measurement procedure for B OUT. Disconnect the test scope and the Calibrator.

5. Check Dot Response Range

Requirement - DOT RESPONSE, a screwdriver adjustment control for each channel has a range of ±5% from unity dot response.

a. Connect the Hi Amplitude output signal from the Type 106 through a 5 ns coaxial cable and a 10X attenuator to the A INPUT connector of the Type 3S1. Connect the trigger output signal from the Type 106 through a coaxial cable and a 5X attenuator to the trigger Ext connector of the Type 3T77A.

b. Change the following controls:

Type 3S1

Display Mode switch	CHAN A
mVOLTS/DIV, Channel A	100
mVOLTS/DIV, Channel B	100

Type 3T77A

Time/div	.2 μsec/div
Dots Per Div	10
Trigger	Ext -

c. Set the Type 106 controls for a 50 kHz repetition rate, and the output amplitude for 5 divisions of display.

d. Adjust the trigger sensitivity of the Type 3T77A for a stable display, and set the Time Position control for no dots along the positive square wave transition as shown in Fig. 7-1.

e. Turn the A DOT RESPONSE screwdriver adjustment control clockwise. The first dot displayed after the positive-going step should be equal to or more than 0.25 division above the flat top of the displayed square wave. See Fig. 7-1A.

f. Turn the A DOT RESPONSE screwdriver adjustment control counterclockwise. The first dot displayed after the positive-going step should be equal to or more than 0.25 divisions below the flat top of the displayed square wave. See Fig. 7-1B.

g. Set the A DOT RESPONSE adjustment so the first dot after the positive-going step is in line with the flat top of the displayed square wave. See Fig. 7-1C.

h. Move the signal cable to B INPUT. Set the Display Mode switch to CHAN B and repeat the procedure for Channel B.

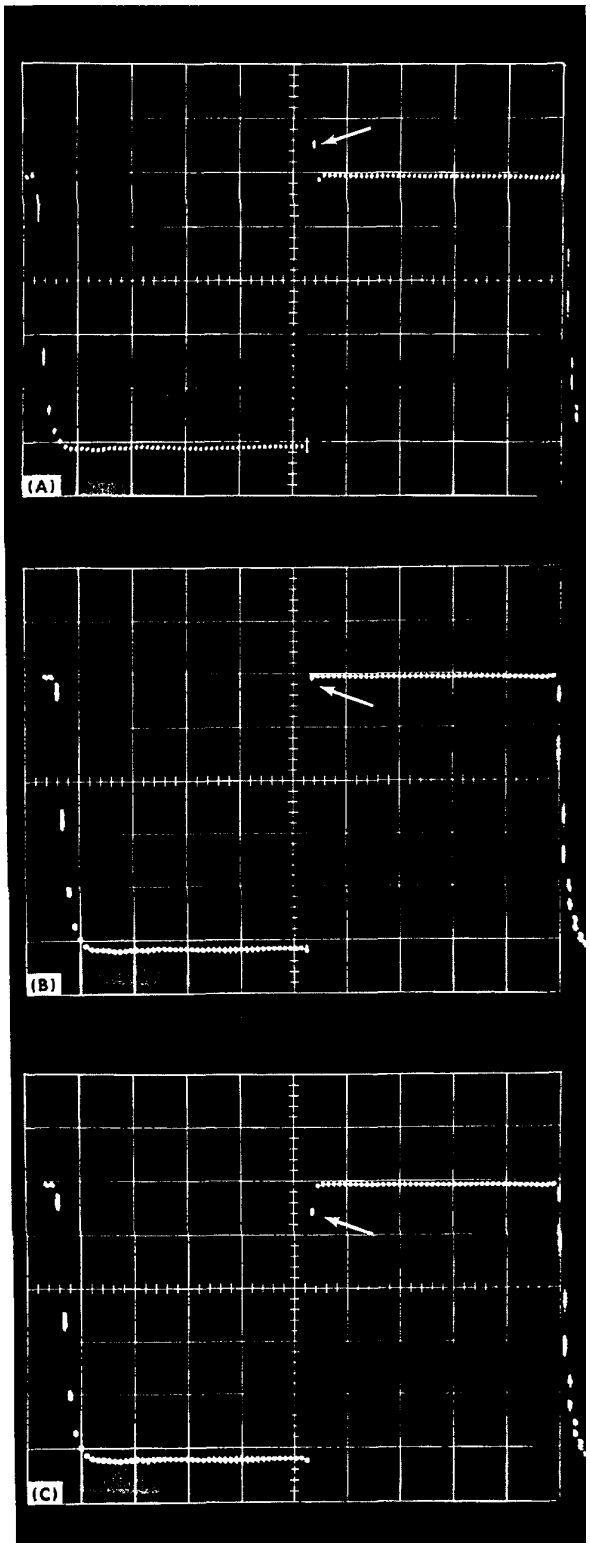

Fig. 7-1. Typical photographs showing Dot Response Range, (A) clockwise, (B) counterclockwise, (C) centered with unity dot response.

6. Check Dot Response in Smooth

Requirement - The Dot Response in SMOOTH position for both channels is ≤0.3:1.

a. Set the SMOOTH-NORMAL switch to the SMOOTH position.

b. Check that the first dot on the step is within 1.5 divisions of the lower flat portion of the waveform. See Fig. 7-2.

c. Move the signal cable to A INPUT and repeat step b.

d. Set the SMOOTH-NORMAL switch to the NORMAL position.

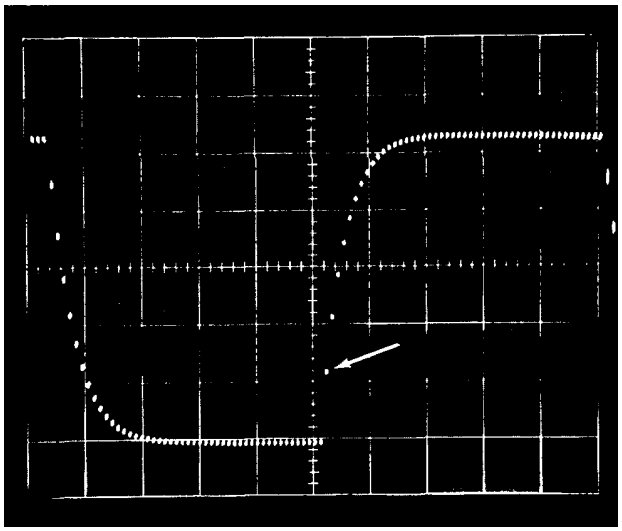

Fig. 7-2. Typical photograph showing dot response in SMOOTH.

7. Check Baseline Shift with Repetition Rate Changes

Requirement - Baseline shift of both channels is ≤10 mV with a repetition rate change from 30 Hz to 100 kHz.

a. Set the mVOLTS/DIV switch to 20.

b. Turn the DC OFFSET control clockwise until the bottom flat portion of the displayed trace is on the center horizontal line of the graticule.

c. Change the repetition rate of the Type 106 from 30 Hz to 100 kHz, and observe that the baseline should not shift vertically more than 10 mV (1/2 minor division).

d. Move the signal input to B INPUT and repeat the procedure for Channel B.

8. Check Dot Slash

Requirement - Dot Slash for each channel is ≤0.1 division of display with a signal repetition rate of 20 Hz.

a. Change the following controls:

Type 3S1

DC OFFSET ±1 V, Channel A	Midrange (5 turns from one end]
DC OFFSET ±1 V, Channel B	Midrange (5 turns from one end)
mVOLTS/DIV, Channel A	200
mVOLTS/DIV, Channel B	200

Type 3T77A

Time/div	2 *m*sec/div
Time Position	Clockwise
Trigger Sensitivity	Clockwise
Trigger	Ext +

b. Set the Amplitude control of the Type 106 for 5 divisions of display, and the repetition rate at 10 kHz.

c. Adjust the trigger controls of the Type 3T77A for a stable display.

d. Change the repetition rate of the Type 106 to 20 Hz, and observe that the vertical excursion of the dot is ≤0.1 division. See Fig. 7-3.

e. Move the signal cable to A INPUT connector. Set the Display Mode switch to CHAN A, and observe that the vertical excursion of the dot is ≤0.1 division.

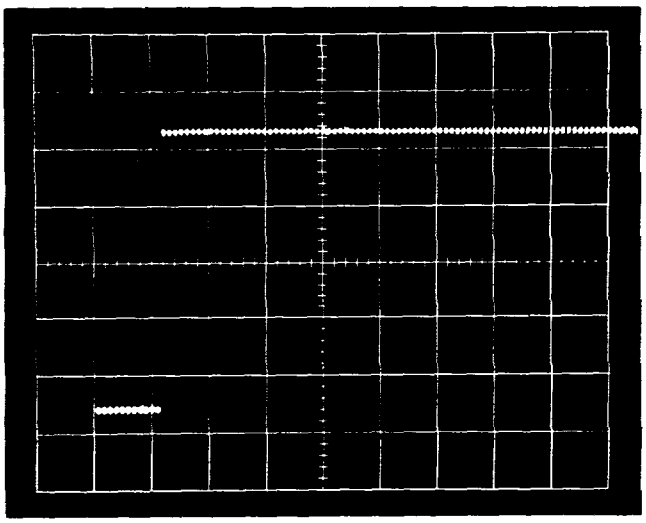

Fig. 7-3. Showing Dot Slash ≤0.1 DIV at 20 Hz (time exposure).

9. Check Tangential Noise

Requirement - Tangential noise for each channel is ≤2 mV in the NORMAL position, and ≤1 mV in the SMOOTH position of the SMOOTH-NORMAL switch.

NOTE

When making a visual noise reading from a sampling display, the eye interprets a noise value which is neither the RMS (root mean square) value nor the peak to peak value. Since most observers agree that a displayed noise value is approximately 3 times its RMS value, it is convenient to define the "tangential noise" value as exactly 3 times its RMS value. The tangential noise value thus defined contains approximately 90% of the trace dots and represents what most people see in the display.

a. Change the following controls:

Type 3S1

mVOLTS/DIV, Channel A	2
mVOLTS/DIV, Channel B	2

Type 3T77A

Time/div	20 nsec/div
Dots Per Div	100
Trigger Sensitivity	Clockwise
Recovery Time	Clockwise

b. Connect the Type 106 Fast Rise Output through a 5 ns 50 Ω coaxial cable and two 10X attenuators to the Type 3S1 A INPUT.

c. Set the Type 106 controls for 100 Hz, and an output amplitude that will cause a display of two parallel lines of noise dots. See Fig. 7-4A.

d. Turn the + Transition Amplitude control counterclockwise until the separation between the two parallel lines of dots is reduced to a point where they appear as one line; that is until the dark band between traces just disappears and the brightness appears constant across the area of both traces. Turn the scale illumination off to see this most clearly. See Fig. 7-4B.

e. Set the Channel A mVOLTS/DIV switch to 50, and remove both attenuators from the signal path, leaving only the 50 Ω coaxial cable connected from Type 106 to the A INPUT connector.

f. Measure the display amplitude in divisions, multiplying the number by 0.75 to obtain the tangential noise of ≤2 mVolts. See Fig. 7-4C.

g. Move the signal to B INPUT. Set the Display Mode switch to B INPUT, and repeat the procedure for Channel B.

NOTE

To calculate the tangential noise, first measure the display amplitude in divisions. Determine the RMS noise amplitude by multiplying the display amplitude by 50 (mV/Div setting) and dividing by 100 (two 10X attenuators) and by a factor of two since the trace separation is twice the RMS noise. Tangential noise is equal to 3 times RMS noise. In simplified form, the tangential noise in mV is equal to 0.75 times the amplitude of the drive signal in divisions at the 50 mV/Div setting with the two 10X attenuators removed.

h. Set the SMOOTH-NORMAL switch to SMOOTH, and repeat steps b through f. The tangential noise in the SMOOTH position is ≤1 mVolt. See Fig. 7-5.

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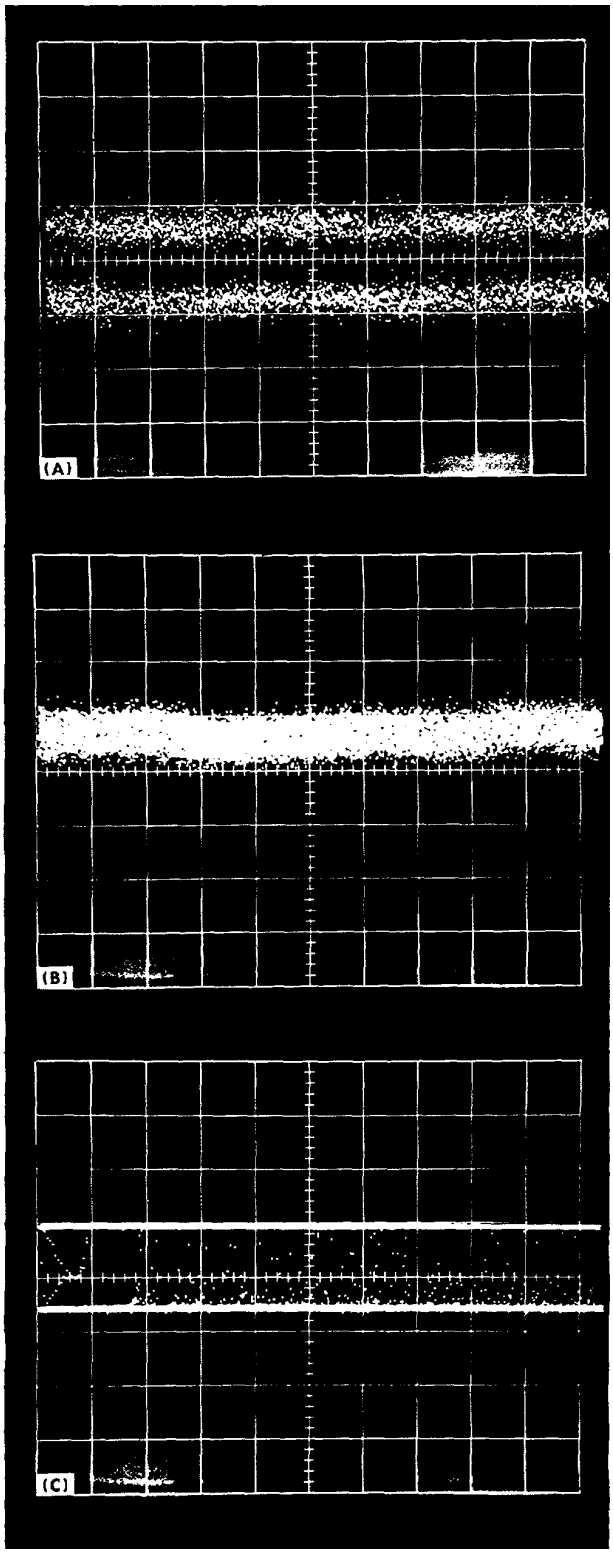

Fig. 7-4. Typical displays (NORMAL position) showing steps used in the measurement of tangential noise, (A) 2 parallel traces, (B) 2 parallel traces joined to appear as one line, (C) equivalent of tangential noise.

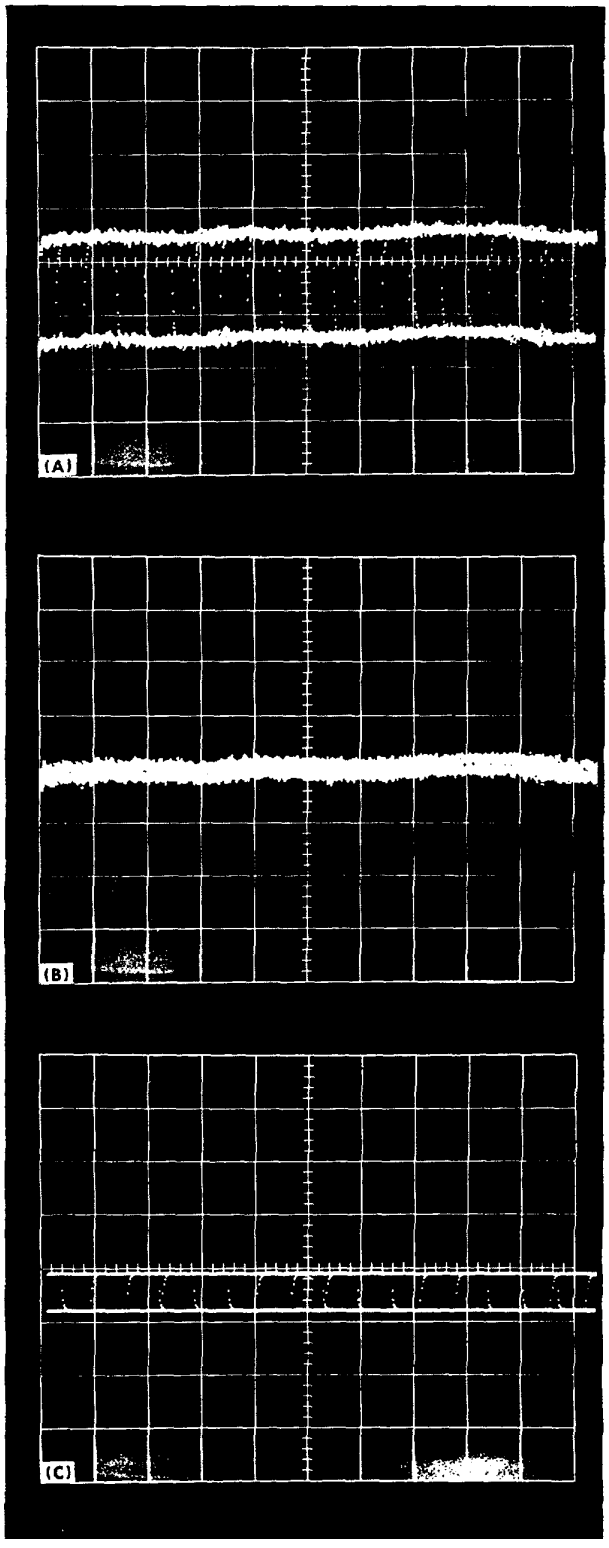

Fig. 7-5. Typical displays (SMOOTH position) showing steps used in measurements of tangential noise.

i. Move the signal to A INPUT. Set the Display Mode switch to A INPUT, and repeat the procedure for Channel A.

j. Disconnect the Type 106.

10. Check Risetime

Requirement - The equivalent risetime of the displayed signal must be 350 ps or less from 10% to 90% amplitude points.

a. Change the following controls.

Type 3S1	
mVOLTS/DIV, Channel A	100
mVOLTS/DIV, Channel B	100
INTERNAL TRIGGER	A

Type 3T77A	
Time/div	1 nsec/div
Time Expander	X10
Trigger Sensitivity	Clockwise
Trigger	Int -

b. Connect the signal Pulse Output of the Fast Rise Pulse Generator through a coaxial air line to the A Input connector of the Type 3S1.

c. Locate the negative-going portion of the displayed waveform on the Type 561A, by adjustment of the Trigger Sensitivity, and Time Position controls on the Type 3T77A.

d. Adjust the amplitude of the display for 5 divisions of vertical display.

e. Read the risetime from the 10% to the 90% points as 350 ps or less. See Fig. 7-6.

f. Move the signal to B INPUT connector and change the INTERNAL TRIGGER to B. Repeat the procedure for Channel B.

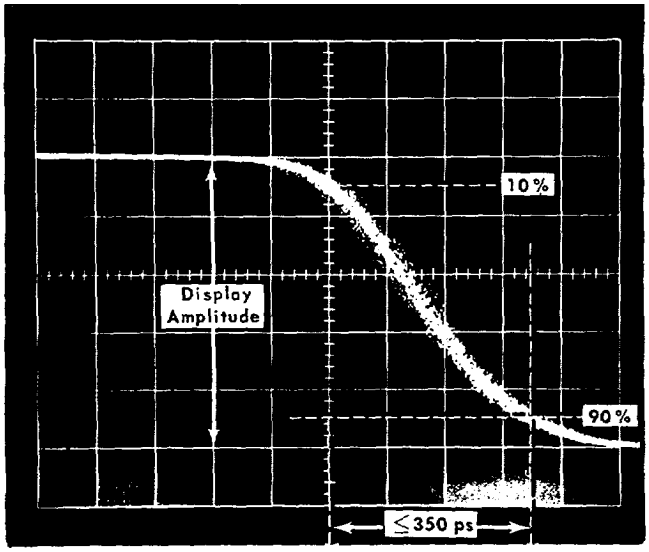

Fig. 7-6. Typical display showing risetime (100 ps/div).

11. Check Interchannel Crosstalk

Requirements - The Interchannel crosstalk is ≤1% P-P using a step signal of ≤80 ps risetime with the observed channel terminated in 50 Ω .

a. Terminate A INPUT with a 50 Ω termination.

b. Set the Display Mode switch to DUAL-TRACE, and the Channel A mVOLTS/DIV switch to 2.

c. Change the Time/div switch on the Type 3T77A to 2 nsec (the Time Expander is at X10).

d. Set the Time Position control of the Type 3T77A and the A and B POSITION controls on the Type 3S1 to obtain a display showing the input signal on Channel B (at 100 mVolts/div) and the interchannel crosstalk signal on the terminated Channel A (at 2 mVolts/div). See Fig. 7-7.

e. Observe that the maximum P-P signal on the Channel A display is ≤1% of the P-P input signal on Channel B.

f. Move the signal to A INPUT connector and the termination to B INPUT. Change the INTERNAL TRIGGER switch to A, and repeat the procedure.

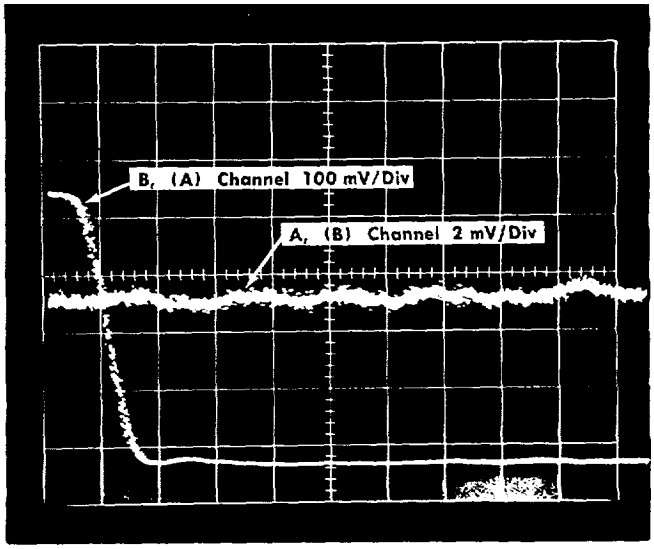

Fig. 7-7. Typical display used to check interchannel crosstalk.

12. Check Co-channel Time Coincidence

Requirement - The equivalent time difference between simultaneous displays of the same waveform on two channels of the Type 3S1 is ≤30 ps.

a. Change the following controls:

Type 3S1	
SMOOTH-NORMAL switch	SMOOTH
mVOLTS/DIV, Channel A	50
mVOLTS/DIV, Channel B	50

Type 3T77A	
Time/div	1 nsec/div

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b. Connect the Pulse Output of the Fast Rise Generator through a Tee connector and two 5 ns coaxial cables to the A INPUT and B INPUT of the Type 3S1.

c. Adjust the Trigger Sensitivity and the Time Position control of the Type 3T77A for a stable trace. Adjust the A and B POSITION controls so that the two traces coincide vertically. See Fig. 7-8A.

d. Measure the time difference between the two channels. It will appear as a horizontal displacement of the vertical portion of one trace as related to the other.

e. Reverse the signal cables to A and B INPUTS, and again measure the time difference between the two channels. If one channel is displayed on the right hand side of the display in both readings, then add the two readings and divide

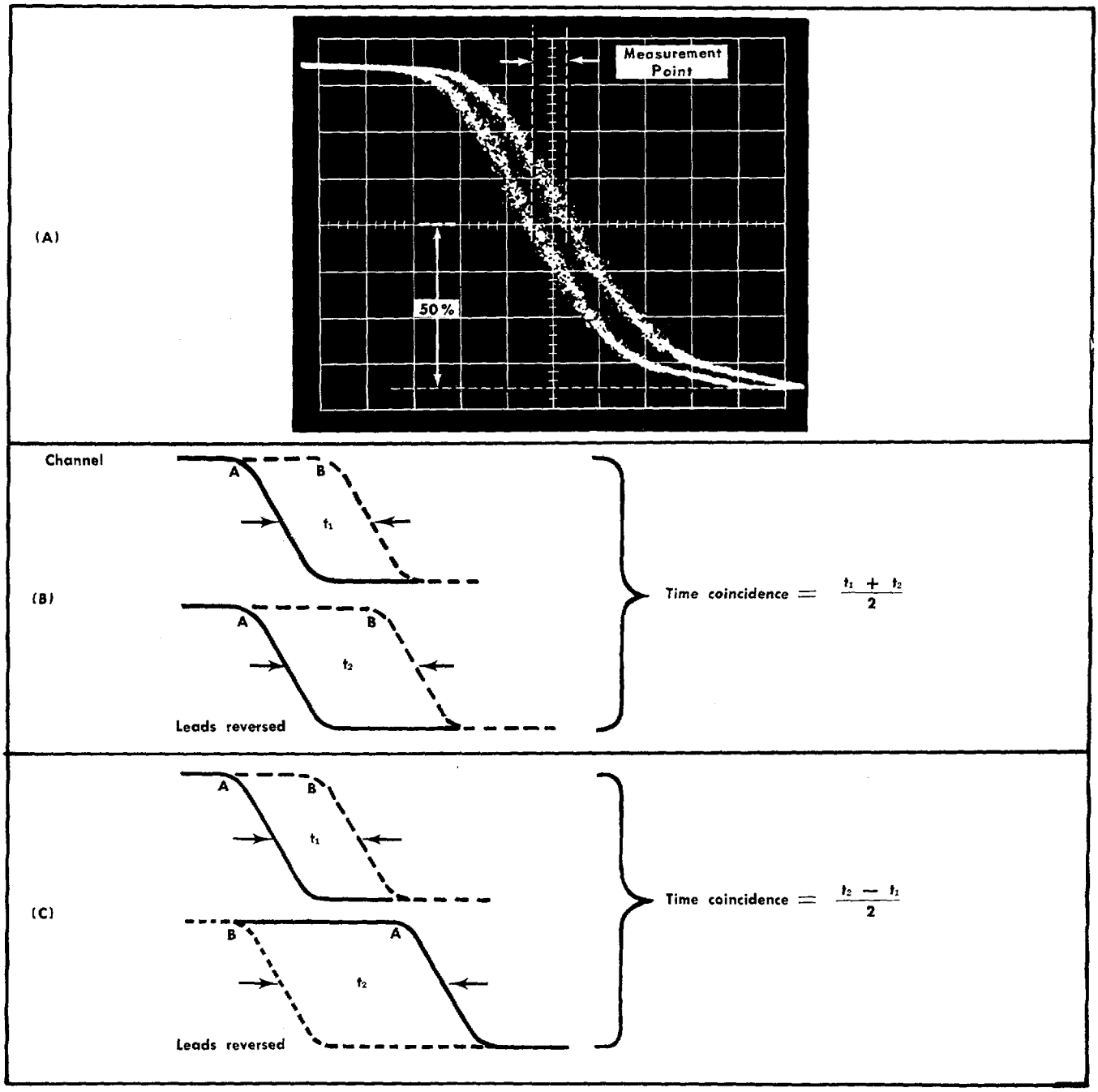

Fig. 7-8. Typical display (A) at 100 ps/division showing one step in checking co-channel coincidence. (B) and (C) drawings show two possible methods of calculating co-channel coincidence.

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by 2, to obtain the time coincidence ≤30 ps. See Fig. 7-8B. If one channel is displaced on the right hand side of the display with one reading, and on the left hand side with the other reading, then divide the difference between the two readings by 2, to obtain the time coincidence ≤30 ps. See Fig. 7-8C. Use the POSITION controls to determine which channel is on the right side of the display.

f. Disconnect the Fast Rise Generator from the Type 3S1.

13. Check Aberration and Tilt

Requirement - The aberration and tilt of a displayed step pulse, after reaching 100%, for each Channel is ≤ plus and minus 2% in the first 5 ns, and ≤ plus and minus 1% after the first 5 ns.

a. Change the following controls:

Type 3S1

Display Mode switch	CHAN A
SMOOTH-NORMAL switch	NORMAL
mVOLTS/DIV, Channel A	200
mVOLTS/DIV, Channel B	200

Type 3T77A

Time/div	2 μsec/div
Time Expander	X1
Time Position	Clockwise
Trigger Sensitivity	Clockwise

b. Connect a Type 281 TDR Pulser to the Type 3S1 A INPUT connector and to the probe power.

c. Adjust the Trigger Sensitivity control on the Type 3T77A for a stable trace. Adjust the A POSITION and the A VARIABLE control on the Type 3S1 for 5 divisions of display, and set the Time Position control on the Type 3T77A for a centered display.

d. Set the Channel A mVOLTS/DIV switch to 10, and turn the A Channel DC OFFSET so the negative portion of the square wave (bottom) of the signal is displayed at the graticule center horizontal line. See Fig. 7-9A.

e. Check the flatness of the display for ≤ plus and minus 1 division vertically (≤ plus and minus 1% of the vertical signal). Note the level of the end of the first division.

f. Set the Type 3T77A Time/div switch to .2 μsec/div, establishing the same reference level at the right edge of the graticule, by using the Type 3S1 A POSITION control if necessary. Use the Time Position control on the Type 3T77A to horizontally move the display.

g. Check the flatness of the display for ≤ plus and minus 1 div vertically (≤ plus and minus 1%), and note the level at the end of the first division. See Fig. 7-9B.

h. Set the Type 3T77A Time/div switch to 20 nsec/div, establishing the some reference level at the right edge of the graticule, by use of the Type 3S1 A POSITION control if necessary. Check the flatness of the display for ≤ plus and minus 1 division vertically (≤ plus and minus 1%). See Fig. 7-9C.

i. Set the Type 3T77A Time/div switch to 2 nsec/div establishing the same reference level at the right edge of the graticule, by use of the Type 3S1 A POSITION control if necessary. Check aberrations of the first 2 1/2 divisions for ≤ plus and minus 2 divisions vertically (≤ plus and minus 2%). See Fig. 7-9D.

j. Change the Type 281 TDR Pulser to the B INPUT connector and the INTERNAL TRIGGER to B. Repeat the procedure for Channel B.

k. Disconnect the Type 281.

14. Check OFFSET OUT (Range and Accuracy)

Requirement - Each channel OFFSET OUT jack is 10 times the DC offset referred to input) ±2%, with an output impedance of 10 kΩ.

a. Change the following controls:

Type 3S1

Display Mode switch	CHAN A
DC OFFSET ±1 V, Channel A	0 Volts at A OFFSET OUT
DC OFFSET ±1 V, Channel B	0 Volts at B OFFSET OUT
mVOLTS/DIV, Channel A	200
mVOLTS/DIV, Channel B	200
VARIABLE mVolts/div (both channels)	CAL

Type 3T77A

Time Position	Midrange
Trigger Sensitivity	Clockwise
Trigger	Ext +

Type 545B

Horizontal Display	A
Horizontal Position	Midrange
Triggering Mode	Auto
Time/cm	5 ms
Variable	Calibrated

Type W Plug-In

Display	A-Vc
Input Atten	R ≈ ∞
Millivolts/cm	20
Variable	Cal
Comparison Voltage	0.00
Vc Range	-11
A Input Selector	DC
Position	Midrange

b. Connect the (Type W) A input through a 1X test probe to A OFFSET OUT jack of the Type 3S1, and adjust the A Channel DC OFFSET ±1 V control for zero volts out as indicated on the Type W.

c. Set the 50 Ω Amplitude Calibrator Volts switch to .6, and connect this output through a 50 Ω coaxial cable to A INPUT connector of the Type 3S1.

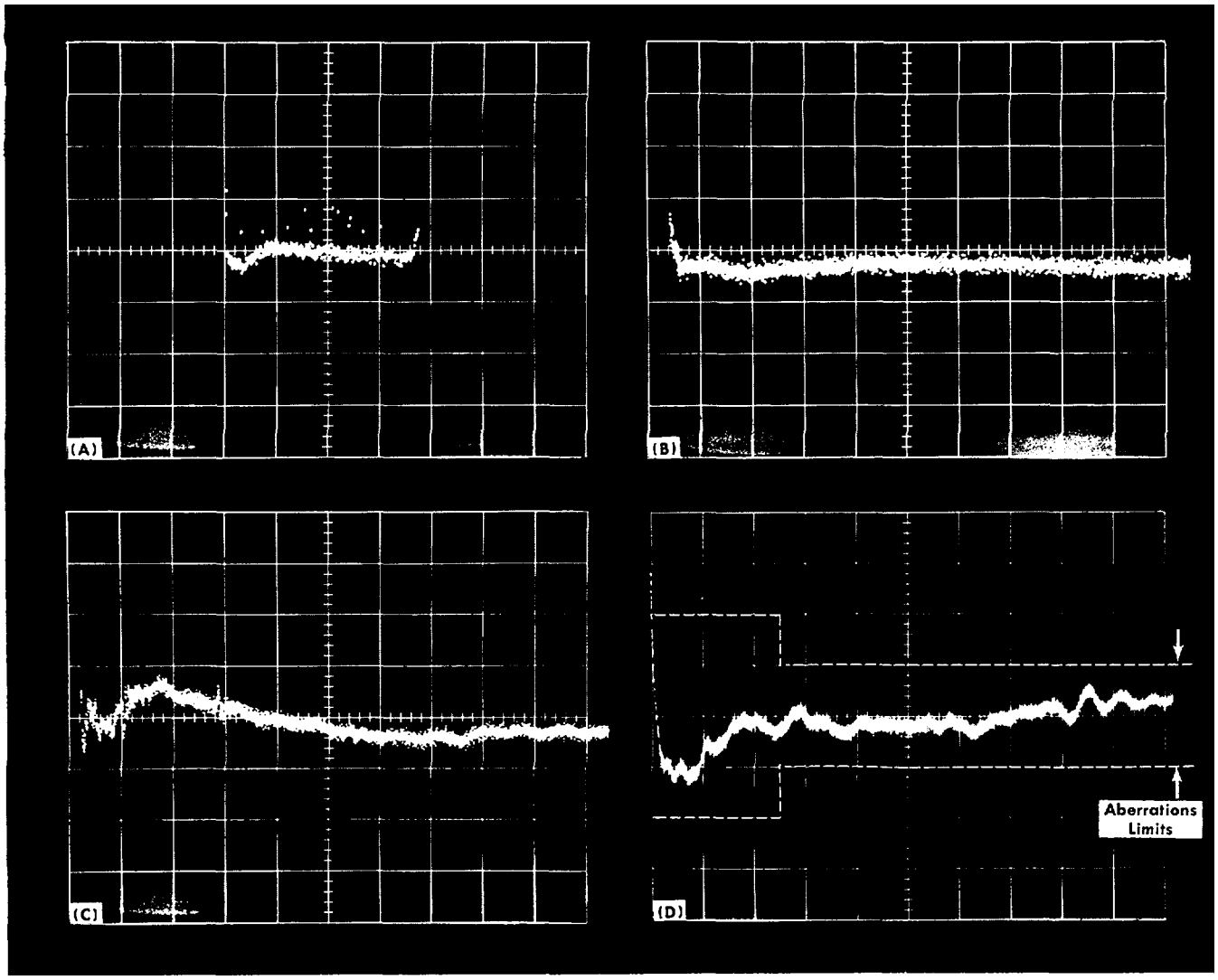

Fig. 7-9. Typical display showing aberration and tilt at (A) 2 msec/div, (B) .2 msec/div, (C) 20 nsec/div, (D) 2 nsec/div.

d. Connect the trigger output signal of the Amplitude Calibrator through a coaxial cable and a 5X attenuator to the Ext Input of the Type 3T77A.

e. Adjust the Trigger Sensitivity of the Type 3T77A for a stable trace, and adjust the Type 3S1 A POSITION control to move the top of the displayed signal to the center of the graticule.

f. Set the A Channel mVOLTS/DIV switch to 5 and use the A POSITION control to set the top of the displayed signal to the center of the graticule.

g. Turn the A Channel DC OFFSET ±1 V control clockwise until the bottom of the signal is displayed at the centerline of the graticule, and measure the offset voltage by adjusting the Comparison Voltage (Vc) of the Type W to 6 Volts ±2%.

h. Set the Comparison Voltage (Vc) of the Type W to 10 Volts, turn A Channel DC OFFSET $\pm$1 V control fully clockwise, and check for $\geq$ -10 Volts.

i. Set the Vc Range switch to +11, turn the A Channel DC OFFSET counterclockwise, and check for $\geq$ +10 Volts.

j. Change the signal input to B INPUT connector, set the Display Mode switch to CHAN B, and connect the test probe to B OFFSET OUT. Repeat the operation for Channel B.

15. Check Vertical Position Indicator

Requirement - One indicator lamp will be on and the other off when a single CRT trace is more than one division above or below the graticule centerline.

a. Disconnect all signals from the Type 3S1 and 3T77A, and set the mVOLTS/DIV switches to 200.

b. Set the Display Mode switch to CHAN A, and position the trace one division above the graticule centerline with the A POSITION control. Observe that the upper position light is on and the lower light is off.

c. Position the trace one division below the graticule centerline with the A POSITION control, and observe that the lower position light is on and the upper light is off.

d. Repeat the above procedure for Channel B.

OPTIONAL CHECKS

Introduction

This part of the performance check is intended for operational checks where maintenance has been performed on the equipment or the particular intended use of the equipment shows a need for these checks.

16. Check A+B (Algebraic addition)

Requirement - With the Amplitude Display switch in the A+B position, the Type 3S1 must add Channel A and B algebraically.

a. Set the controls as follows:

Type 3S1

Display Mode switch	CHAN A
SMOOTH-NORMAL switch	NORMAL
A POSITION	Midrange
B POSITION	Midrange
DC OFFSET ±1 V, Channel A	Midrange (5 turns from one end)
DC OFFSET ±1 V, Channel B	Midrange (5 turns from one end)
mVOLTS/DIV, Channel A	200
mVOLTS/DIV, Channel B	200
VARIABLE mVolts/div (both channels)	CAL
INVERT-NORM switch, Channel A	NORM
INVERT-NORM switch, Channel B	NORM
INTERNAL TRIGGER	OFF
HORIZ PLUG-IN	SAMPLING 3T-SERIES

Type 3T77A

Horizontal Position	Midrange
Time/div	2 μsec/div
Time Expander	X1
Time Position	Clockwise
Dot Per Div	100
Trigger Sensitivity	Clockwise
Sweep Mode	Normal

b. Connect a signal from the 50 Ω Amplitude Calibrator through a tee and two 5 ns coaxial cables to A INPUT and B INPUT connectors. Set the Volts switch on the 50 Ω Amplitude Calibrator to .6 and observe two divisions of display through Channel A.

c. Set the Display Mode switch to CHAN B, and observe two divisions of display.

d. Set the Display Mode switch to the A+B position and observe a 4 division display. Adjustment of the A and B POSITION controls may be necessary.

e. Set the INVERT-NORM switches to INVERT (both channels) and observe 4 divisions of display.

f. Set the INVERT-NORM switch of Channel A to NORM and observe a minimum amplitude display showing +A -B.

17. Check A VERT B HORIZ display

Requirement - With the Amplitude Display switch in the A VERT B HORIZ position, and using the horizontal amplifier of the Sampling Sweep plug-in unit, the Type 3S1 must plot the A Channel vertically and the B Channel horizontally to form an X-Y display on the CRT.

a. Set the Display Mode switch to the A VERT B HORIZ position.

b. Observe an X-Y display of the signal on Channel A vertically and the signal on Channel B horizontally forming an angle of 45 degrees from the horizontal line.

18. Check Digital Logic (with Readout System)

Requirement - With the VARIABLE controls of each channel in the CAL (detent) position, one decimal and the unit lamps on the Type 6R1A must be lighted to indicate the proper decimal and the units with the selection of the mVOLTS/DIV switch positions. All decimal and unit lamps will be out when the indicated Channel VARIABLE control is not in the CAL (detent) position.

a. Plug the Type 3S1 into the left compartment of the Type 567 Oscilloscope. Plug the Type 3T77A into the center compartment, and the Type 6R1A into the right hand compartment. Turn the Power switch on and allow a 20-minute warm up.

b. Set controls as follows:

Type 3S51

Display Mode switch	CHAN A
SMOOTH-NORMAL switch	NORMAL
A POSITION	Midrange
B POSITION	Midrange
DC OFFSET, Channel A	Midrange (5 turns from one end)
DC OFFSET, Channel B	Midrange (5 turns from one end)
mVOLTS/DIV, Channel A	200
mVOLTS/DIV, Channel B	200
Variable mVolts/div (both channels)	CAL
INVERT-NORM switch, Channel A	NORM
INVERT-NORM switch, Channel B	NORM
INTERNAL TRIGGER	B
HORIZ PLUG-IN	SAMPLING 3T-SERIES

Type 6R1A

Mode switch	Voltage A
B Voltage switch	down position
A Voltage switch	down position
Resolution switch	Hi
Display Time	Midrange

c. Change the VARIABLE control and the mVOLTS/DIV switch for Channel A in the steps as shown in Table 7-2, and check the units and the position of the decimal lamps to be lighted.

d. Change the Display Mode switch on the Type 3S1 to CHAN B. Change the Mode switch on the Type 6R1A to Voltage B, and complete the same procedure for Channel B.

e. Reset mVOLTS/DIV switches for both channels to 200.

TABLE 7-2

VARIABLE control	mVOLTS/DIV switch position	Decimal	Units
uncal	any	0 0 0 0 0	
CAL	200	0 0 X 0 0	V
CAL	100	0 0 0 0 X	MV
CAL	50	0 0 0 0 X	MV
CAL	20	0 0 0 0 X	MV
CAL	10	0 0 0 X 0	MV
CAL	5	0 0 0 X 0	MV
CAL	2	0 0 0 X 0	MV

19. Check Vertical Digital Accuracy (with Readout System)

Requirement - The Type 3S1 will make vertical digital measurements with a readout system such as Tektronix Types 567, 6R1A and 3T77A or Types 568, 262 and 3T77A with an accuracy of ±3%.

a. Connect the 50 Ω Amplitude Calibrator signal through a 5 ns coaxial cable to the B INPUT connector of the Type 3S1, and set the 50 Ω Amplitude Calibrator Volt switch to .6.

b. Turn the Trigger Sensitivity control for a stable display, and adjust the B 0% Zone control on the Type 6R1A so its intensified zone is at the top of the displayed square wave. Slight adjustment of the Intensity control on the Type 567 may be necessary to show the intensified zones.

c. Adjust the B 100% Zone control on the Type 6R1A so its intensified zone is at the negative portion (bottom) of the displayed square wave following the negative step.

d. Observe a reading of 0.6V ±3%.

e. Change the Display Mode switch to CHAN A, and the INTERNAL TRIGGER switch to A on the Type 3S1. Change the Mode switch on the Type 6R1A to Volt age A, and repeat the procedure for Channel A by adjusting the A 0% and 100% Zone controls.

20. Check Real Time Operation (with Readout System)

Requirement - The Type 3S1 will make real time measurements with a readout system such as Tektronix Types 567, 6R1A and 382 or Types 568, 262 and 3B2 in the following positions of the Display Mode switch; CHAN A, DUAL-TRACE, AND CHAN B. Real time measurements do not apply in the A+B or the A VERT B HORIZ positions of the Display Mode switch.

a. Plug the Type 3S1 into the left compartment of the Type 567 Oscilloscope. Plug the Type 3B2 into the center compartment, and the Type 6R1A into the right hand compartment. Turn the Power switch on and allow a 20-minute warm up.

b. Using the internal calibrator of the Type 567, connect the 500 mV output through a 50 Ω coaxial cable and a GR adapter to the A INPUT connector of the Type 3S1. Set the internal calibrator to the ≈1 kc position, and connect the + Pretrigger signal through a coaxial cable to the Ext Trig In connector of the Type 3B2.

c. Set controls as follows:

Type 3S1

Display Mode switch	CHAN A
SMOOTH-NORMAL switch	NORMAL
A POSITION	Midrange
B POSITION	Midrange
DC OFFSET, Channel A	Midrange (5 turns from one end)
DC OFFSET, Channel B	Midrange (5 turns from one end]
VARIABLE mVolts/div (both channels)	CAL
INVERT-NORM switch, Channel A	NORM
INVERT-NORM switch, Channel B	NORM
INTERNAL TRIGGER	OFF
HORIZ PLUG-IN	NON-SAMPLING 2B, 38-SERIES

Type 3B2

Trigger Level	Midrange
Coupling	AC Slow
Slope	+
Source	Ext
Delay Time	10 μs X100
Position	Midrange
Time/div	.2 msec
Digital Resolution	10 μs

Type 6R1A

Mode switch	Time Stop -Start
B Voltage slide switch	negative slope (down)
A Voltage slide switch	negative slope (down]
Resolution	Hi
Start, First-second switch	First
Start, Slope +, - switch	-
Timing Start switch	A Trace 50%
Stop, Slope +, - switch	+
Timing Stop switch	A Trace 50%
Memory Zones-off switch	Memory Zones
Start to Stop-off switch (CRT Intensification)	Off

d. Adjust the Trigger Level and the Position controls on the Type 3B2 for a stable display of 5 divisions.

e. Adjust the A 0% Zone control on the Type 6R1A so the displayed intensified zone is located on the upper portion of the first displayed square wave.

f. Adjust the A 100% Zone control so the displayed intensified 100% zone is located on the lower portion of the displayed square wave following the 0% intensified location.

g. Readout on the Type 6R1A will measure 1/2 cycle of the square wave, or about 0.5 MS.

h. Change the Mode switch on the Type 6R1A to Voltage A, and read the amplitude of the signal of 500 mV ±3%.

i. Change the input signal to B INPUT and repeat the above procedure for Channel B after changing the following controls: the Display Mode switch on the Type 3S1 to CHAN B; the Mode switch on the Type 6R1A to Time Stop-Start; the Timing Start switch on the Type 6R1A to B Trace 50%; the Timing Stop switch to the Type 6R1A to B Trace 50%.

21. Check Real Time Operation (with Real Time Sweep)

Requirement - With the SAMPLING MODE switch in the FREE RUN position, the Type 3S1 will sample the input signal at a 100 kHz ±5% rate, and provide an internal reconstructed trigger signal for use with a real time base plug-in such as Types 2B67, 3B1, 3B2, 3B3, 3B4 and 3B5.

a. Plug the Type 3S1 into the left compartment of the Type 561A Oscilloscope. Plug the Type 2B67 into the right hand compartment. Turn the Power switch on and allow a 20 minute warm up.

b. Set controls as follows:

Type 3S1

Display Mode switch	CHAN A
SMOOTH-NORMAL	NORMAL
A POSITION	Midrange
B POSITION	Midrange
DC OFFSET ±1 V, Channel A	Midrange (5 turns from one end)
DC OFFSET ±1 V Channel B	Midrange (5 turns from one end)
VARIABLE mVolts/div (both channels)	CAL
INVERT-NORM switch Channel A	NORM
INVERT-NORM switch, Channel B	NORM
INTERNAL TRIGGER	A
HORIZ PLUG-IN	NON-SAMPLING 28, 3B-SERIES

Type 2B67

Position	Midrange
Time/div	.2 msec

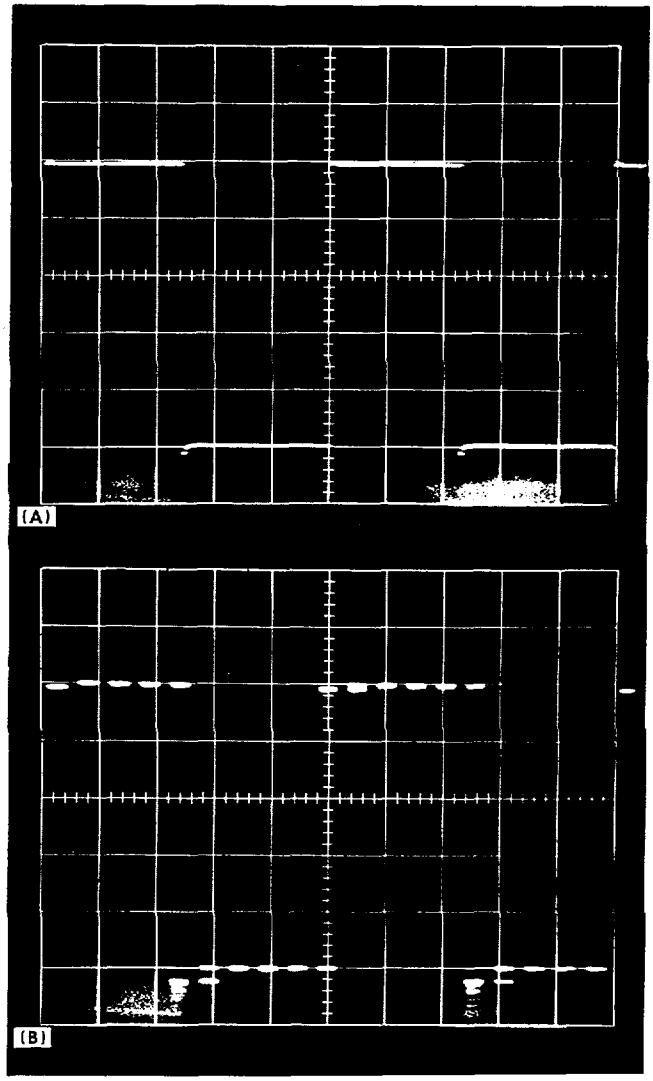

Fig. 7-10. Real time display (A) 1 kHz square wave with a sweep of 0.2 ms/div, (B) 10 kHz square wave with a sweep of 20 ms/div.

Mode switch	Normal
Triggering Level control	Free Run
Triggering Slope	+
Triggering Coupling	AC Slow
Triggering Source	Int

c. Connect the Type 106 Hi Amplitude output through a 5 ns coaxial cable and a 10X attenuator to the A INPUT connector of the Type 3S1. Set the Repetition Rate Range switch and Multiplier of the Type 106 for 1 kHz. Set the Hi Amplitude-Fast Rise switch to Hi Amplitude, and adjust the output amplitude control for a display of 5 divisions.

d. Adjust Triggering Level control of the Type 2B67 for a stable trace. See Fig. 7-10A.

e. Set the Repetition Rate Range switch and the Multiplier of the Type 106 for 10 kHz. Set the Time/div switch on the Type 2B67 to 20 μsec/div. Observe that the number of samples (2 per horizontal division or 100 kHz ±5% rate) limits the displayed information. See Fig. 7-10B.

f. Change the input signal to B INPUT, and repeat the procedure for Channel B after changing the following controls: Change the Display Mode switch to CHAN B, and the INTERNAL TRIGGER switch to B on the Type 3S1; change the Time/div switch to .2 msec, and the Triggering Level control to Free Run on the Type 2B67.

This concludes the Performance Check of the Type 3S1. If the instrument has met each of the preceding requirements, it will perform to all advertised specifications.

SECTION 8

MAINTENANCE CALIBRATION [1]

Introduction

This calibration procedure can be used for complete calibration of the Type 3S1 to return it to the original performance limits stated in Section 1 of this manual. Completion of every step in this procedure returns the Type 3S1 to original factory performance standards.

General Information

Any needed maintenance should be performed before proceeding with calibration. Troubles which become apparent during calibration should be corrected using the techniques given in the Maintenance section.

This procedure is arranged in a sequence which allows the Type 3S1 instrument to be calibrated with the least interaction of adjustments.

The location of test points and adjustments is shown in each step. Waveforms which are helpful in determining the correct adjustment or operation are also shown.

EQUIPMENT REQUIRED

The equipment listed below and shown in Fig. 8-1 and Fig. 8-2, or its equivalent, is required for a complete recalibration of the Type 3S1 Dual-Trace Sampling Unit. Equipment specifications given are the minimum necessary for the particular use of each item. All test equipment must be correctly calibrated and functioning properly. If equipment is substituted, it must meet or exceed the limits stated below.

Some special test equipment items listed are suggested for the most accurate and fastest calibration. All equipment listed, except items 20, 23 and 24 can be obtained by ordering through your local Tektronix Field Engineer or Representative.

1. Test Oscilloscope. Bandwidth, DC to about 20 MHz. Minimum deflection factor of 5 mV/div, offset by up to 11 volts DC (calibrated to ±0.2%). Tektronix Type 545B Oscilloscope with Type W Plug-In Unit suggested.

2. 10X Probe for use with test oscilloscope. Tektronix P6012 Probe. Tektronix Part No. 010-0203-00.

3. 1X Probe for use with test oscilloscope. Tektronix P6011 Probe. Tektronix Part No. 010-0193-00.

4. Special flexible Plug-In Extension cable, for operating the Type 3S1 outside the indicator oscilloscope. Tektronix Part No. 012-0066-00 required.

5. Indicator Oscilloscope such as the Tektronix Type 561A used in the following procedure (or other indicator in which the Type 3S1 is normally operated).

6. Type 3T77A Sampling Sweep Unit, as used in the following procedure, or other Timing Unit normally used with the Type 3S1.

7. Special Tektronix 50 Ω Amplitude Calibrator. Square wave output signal at approximately 40 kHz; amplitudes of 0.012 to 1.2 volts in seven steps, at ±0.25% when loaded by 50 Ω. Tektronix Calibration Fixture, Part No. 067-0508-00.

8. Tunnel Diode Pulse Generator. Risetime must be ≤80 ps 10% to 90% at approximately 400 mV into 50Ω. Special Tektronix Calibration Fixture, Part No. 067-0513-00.

9. 50 Ω In-Line Pulse Generator. Tektronix Type 281 TDR Pulser required because of known waveshape and transient response.

10. Variable-Frequency Square-Wave Generator. Risetime less than 15 ns, amplitude approximately zero to 600 mV into 50 Ω. Frequencies used: 20 Hz, 30 Hz, 100 Hz and 100 kHz. Tektronix Type 106 Square-Wave Generator suggested.

11. Two 50 Ω 10X Coaxial Attenuators, such as GR 874-G20. Tektronix Part No. 017-0078-00.

12. One 50 Ω 5X Coaxial Attenuator, such as GR 874-G14. Tektronix Part No. 017-0079-00.

13. One 50 Ω 2X Coaxial Attenuator, such as GR 874-G6. Tektronix Part No. 017-0080-00

14. 50 Ω End-Line Termination, such as GR 874-W50B. Tektronix Part No. 017-0081-00.

15. 20 cm coaxial line, such as GR 874-L20. Tektronix Part No. 017-0084-00.

16. GR 874 to BNC male connector adapter, such as GR 874-QBJA. Tektronix Part No. 017-0064-00.

17. GR 874-T, Tee connector, 50 Ω. Tektronix Part No. 017-0069-00.

18. Two identical quality 50 Ω coaxial cables. RG 213/U, 5 ns signal delay, with GR 874 connectors. Tektronix Part No. 017-0502-00.

19. 50 Ω coaxial cable, RG 58C/U, 10 ns signal delay, with GR 874 connectors. Tektronix Part No. 017-0501-00.

20. DC Bridge for measuring 50 Ω. Plus or minus 2 volts DC maximum across 50 Ω resistor. Accuracy, 0.2% required.

21. Plastic tool for adjusting Blow-By Capacitors. Tektronix Part No. 003-0334-00.

22. Plastic tool for adjusting ferrite slug of L24, 5/64, inch inside diameter hex core. Tektronix Part No. 003-0310-00. Handle for 003-0310-00, Tektronix Part No. 003-0307-00.

23. Small insulated handle, 5/64, inch bit screwdriver for adjusting screwdriver-adjust controls. (Not shown.)

24. An RMS reading line voltage meter, with a ±3% accuracy at the line voltage to which the indicator oscilloscope is connected. (Not shown.)

[1] This procedure is for use after repair only. For calibration procedure, see TB 750-236.

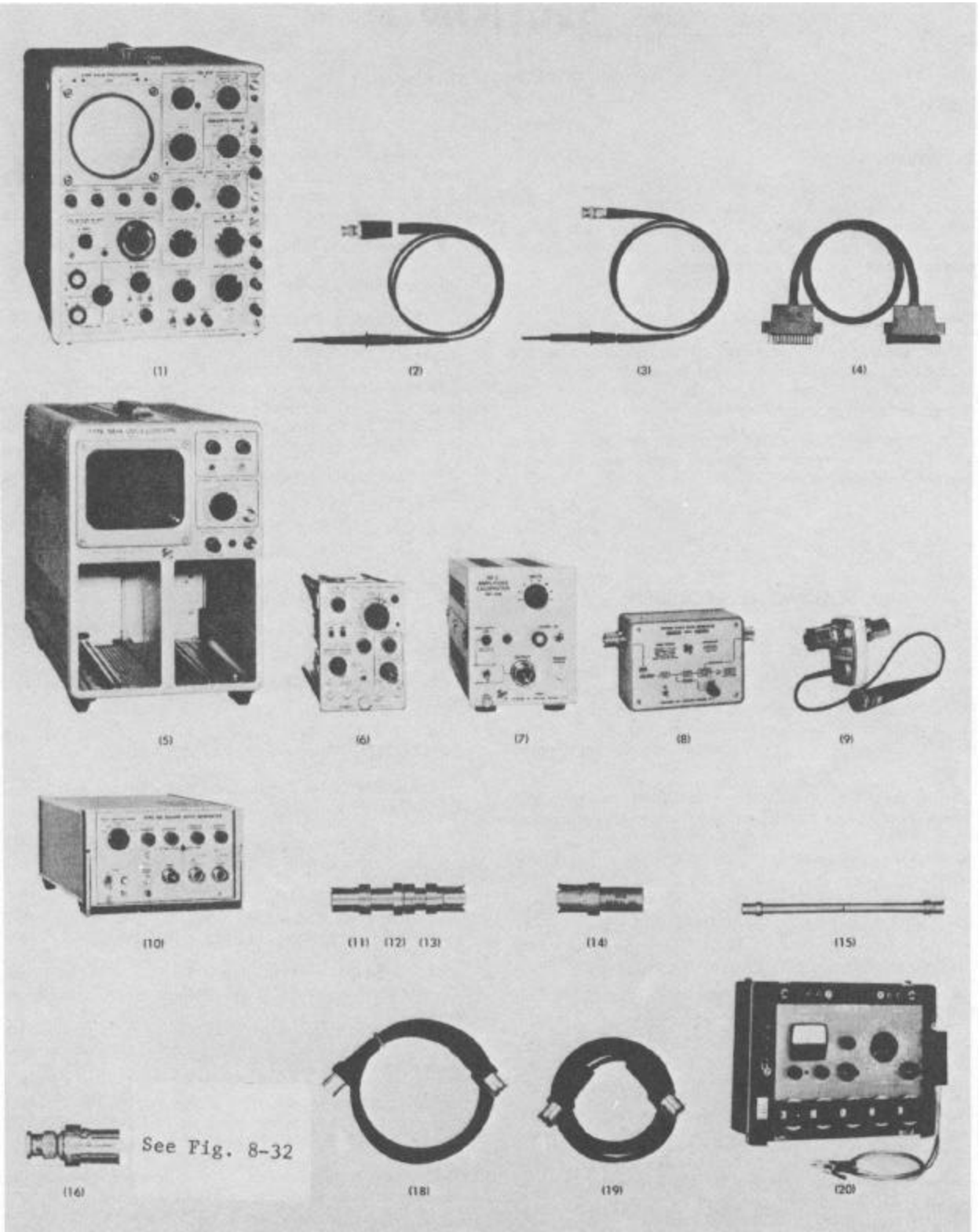

Fig. 8-1. Calibration equipment.

Fig. 8-2. Calibration alignment tools.

CALIBRATION RECORD AND INDEX

The following abridged Calibration Procedure may be used as a calibration guide by the experienced calibrator, or it may be used as a calibration record. (The abridged procedure may be reproduced without special permission of Tektronix, Inc.) The step numbers and titles are identical to those used in the complete procedure. When the whole procedure is performed, the Type 3S1 will meet all Characteristics listed in Section 1 of this manual.

Type 3S1 Serial No. _____
Calibration Date _____
Calibrated By _____

PRELIMINARY PROCEDURE

CALIBRATION PROCEDURE

- ☐ 14. Adjust Inverter Zero Controls — Page 8-21
  Chan A: R283 Chan B: R583
- ☐ 15. Adjust Internal Digital Gain Controls — Page 8-23
  Chan A: R301 Chan B: R601
- ☐ 16. Check A OUT and B OUT Signals (AC Signal Only, Not DC) — Page 8-23
- ☐ 17. Check VERT GAIN Control Range and set VERT GAIN Control (R764) — Page 8-24
- ☐ 18. Adjust A-B Bal Control (R756) (Channel A Vert Gain) — Page 8-25
- ☐ 19. Check mVolts/Div VARIABLE Controls Range and UNCAL Lamps — Page 8-25
  Chan A Chan B
- ☐ 20. Adjust Vertical Centering (R766) and Check Vertical Position Indicating Lamps — Page 8-25
- ☐ 21. Check and Adjust 100 kHz Free Run Frequency (L24) — Page 8-26
- ☐ 22. Check Offset Circuit Operation — Page 8-29
  Chan A Chan B
- ☐ 23. Check Internal Trigger Pickoff Signal Amplitude — Page 8-29
  Chan A Chan B
- ☐ 24. Check Trace Baseline Shift, 100 kHz to 30 Hz — Page 8-30
  Chan A Chan B
- ☐ 25. Check Memory Slash (Dot Drift) at 20 Hz — Page 8-31
  Chan A Chan B
- ☐ 26. Check Interchannel Crosstalk — Page 8-32
- ☐ 27. Check Co-Channel Time Coincidence — Page 8-33
- ☐ 28. Check Tangential Noise — Page 8-36
  Chan A Chan B

NOTES

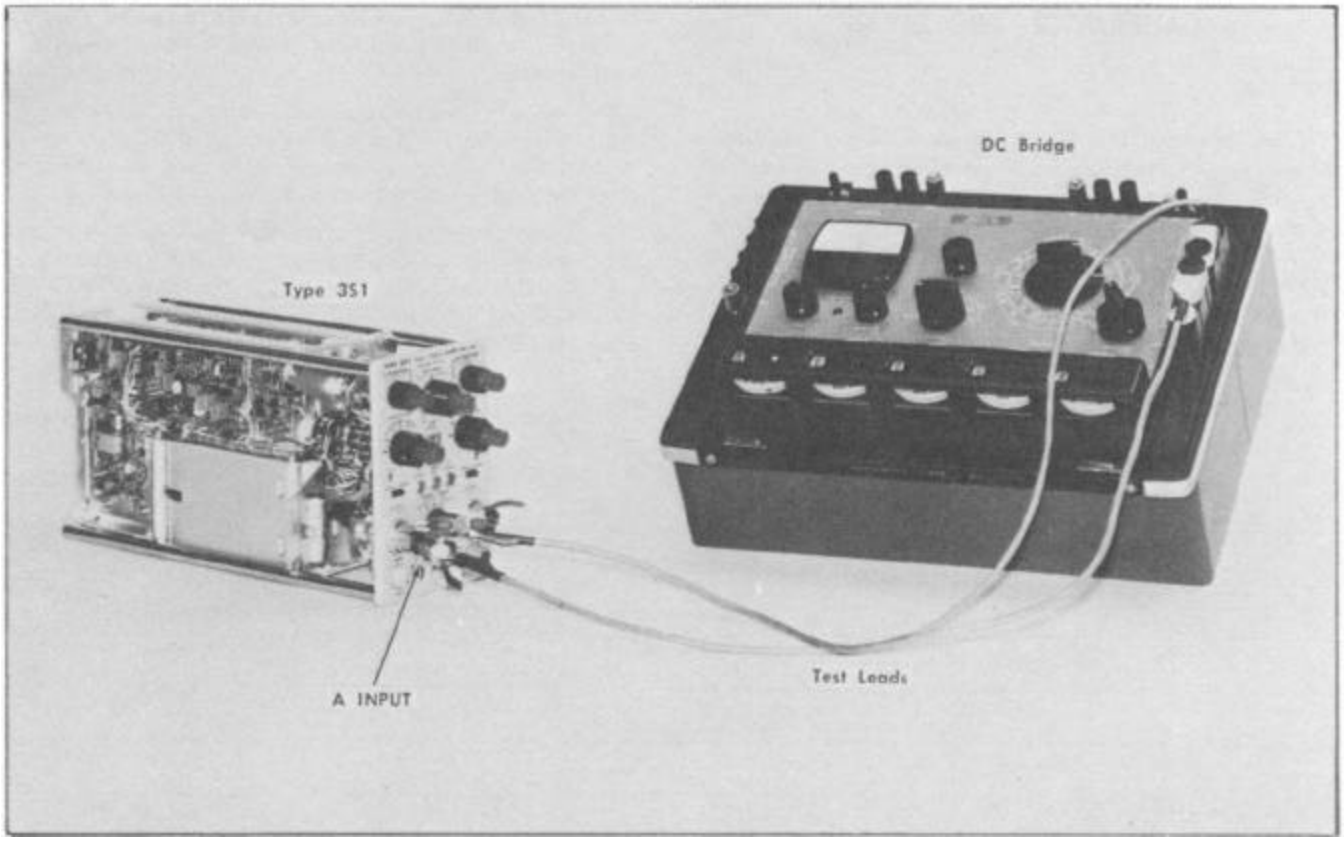

Fig. 8-3. Test equipment setup for Preliminary Procedure, Step 1.

Control Settings

Type 3S1	
INTERNAL TRIGGER	OFF
All other controls	Optional

PRELIMINARY PROCEDURE

1. Check Type 3S1 DC Input Resistance

With the Type 3S1 separated from the indicator oscilloscope, use the DC Resistance Bridge and measure the DC input resistance of both channels. Make certain the bridge does not apply more than ±2 volts to the input terminals.

Set the controls as listed under Fig. 8-3, and connect the bridge leads, one to the frame and the other to the A INPUT connector center pin. Measure the Channel A resistance and record it in the Calibration Record and Index. Tolerance is 50 Ω, ±1 ±Ω.

Change the bridge lead from the A INPUT to the B INPUT connector center pin. Measure the Channel B resistance and record it in the Calibration Record and Index. Tolerance is 50 Ω, ±1 Ω.

Set the INTERNAL TRIGGER switch to A. Remeasure the Channel A input resistance. Record the value in the Calibration Record and Index.

Set the INTERNAL TRIGGER switch to B. Again measure the Channel B input resistance. Record the value in the Calibration Record and Index.

2. Connect the Type 3S1 to the Indicator Oscilloscope

Use the Flexible Plug-in Extension cable, and connect the Type 3S1 to the indicator oscilloscope. Place the cable between the rear horizontally mounted interconnecting plug, and the indicator horizontally mounted interconnecting plug.

CAUTION

Incorrectly connecting the extension cable to the vertically mounted interconnecting plug will cause damage to the Type 3S1, and may cause damage to the indicator oscilloscope when the power is turned on.

Turn the indicator oscilloscope Intensity control fully counterclockwise. Connect the indicator oscilloscope to the correct power source, check the voltage with the RMS AC Voltmeter and turn the Power switch on. Allow a twenty minute warm up before starting the main Calibration Procedure.

During warm up, set the instrument controls as listed following Fig. 8-4.

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CALIBRATION PROCEDURE

General

In the following calibration procedure, a test equipment setup is shown for each major setup change. Control settings are listed following the picture. Controls which are to be changed from a previous setting are printed in bold type. If only a partial calibration is performed, start with the nearest setup preceding the desired step.

NOTE

Do not preset internal controls to midrange as a preliminary to recalibration. When performing a complete recalibration, best performance will be obtained if each adjustment is made to the exact setting, even if the Check is within the allowable tolerance.

The following procedure uses the particular items of equipment listed in the Equipment Required list. If substitute equipment is used, control settings or setup must be altered to meet the requirements of the equipment substituted.

Type 3S1 Units below SN B050740 have the Red HORIZ PLUG-IN control labeled SAMPLING MODE. The two control positions related to the knob, NON-SAMPLING 2B, 3B-SERIES and SAMPLING 3T-SERIES are labeled FREE RUN and TRIGGERED, respectively. Wherever text references are made to the above control, these changes should be noted.

NOTES

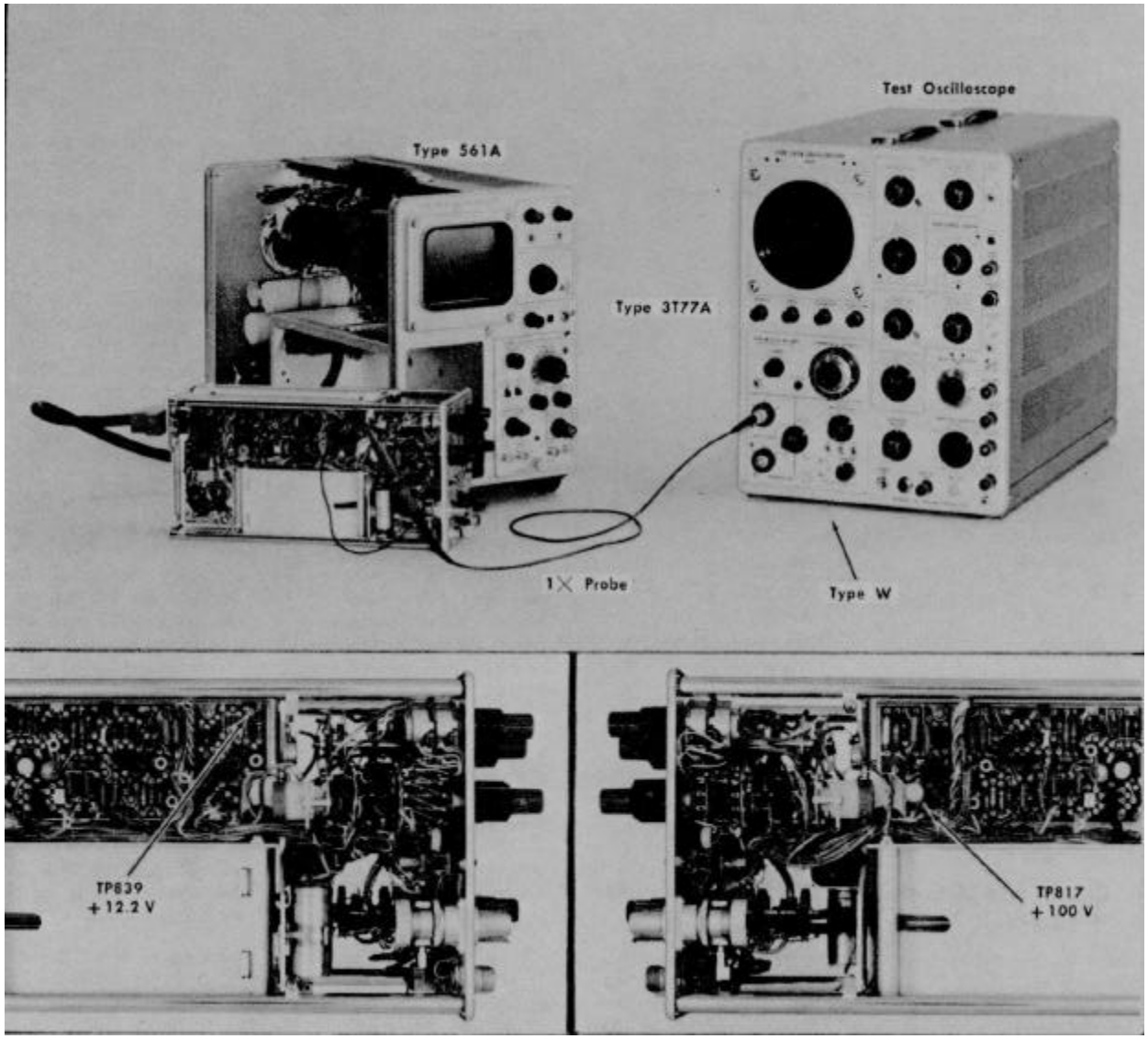

Fig. 8-4. Test equipment setup and Test Points for Steps 1 and 2 of Calibration Procedure.

Control Settings

Type 3S1

Display Mode Switch	CHAN A
SMOOTH-NORMAL	NORMAL
INTERNAL TRIGGER	OFF
HORIZ PLUG-IN	SAMPLING 3T-SERIES

Channel A

A POSITION	Midrange
DC OFFSET	Midrange (5 turns from either end)
m/VOLTS/DIV	100
VARIABLE	CAL
INVERT-NORM	NORM

Channel B

B POSITION	Midrange
DC OFFSET	Midrange (5 turns from either end)
m/VOLTS/DIV	100
VARIABLE	CAL
INVERT-NORM	NORM

Type 3T77A

Horizontal Position	Midrange
Time/Div	1 mSec
Variable	Calib detent position
Time Expander	X1
Dots/Div	100
Time Position	Optional

Ⓐ 1

Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	Fully Counterclockwise
Triggering Source	- Int
Recovery Time	Fully Counterclockwise; pushed in

Test Oscilloscope (if not using precision voltmeter)

Sweep Rate	5 mSec/Div
Triggering	+ Line

Type W

Vc Range	0
Comparison Voltage	(1.220)
Outer Dial	1
Variable Dial	2.20
A Input Coupling	Gnd
Input Atten	10
Display	A-Vc
Millivolts/Cm	5
Variable	Calib detent position
DC Bal	Adjust after 20 minutes warm up
Position	Trace to graticule centerline

Connections

Place the 1X Probe into the A input connector of the Type W. Connect the probe ground clip conveniently near the Type 3S1 Test Point 839 (see Fig. 8-4) and the probe tip at TP839.

1. Check and Adjust Type 3S1 +12.2-Volt Supply

a. Make the probe connection and control settings listed following Fig. 8-4. The test oscilloscope CRT deflection factor is 50 mV/Cm using the control settings listed. The graticule centerline represents +12.2 volts, and 1% is 122 mV or 2.42 divisions up or down from the graticule center.

NOTE

Use this procedure only if a precision voltmeter is not available. If using a voltmeter, place the test lead on TP839, and adjust R832 for precisely +12.2 volts.

b. With the probe connected, the A Input Coupling switch and the Vc Range switch of the Type W must be changed to:

A Input Coupling	DC
Vc Range	+11

Change both switches at the same time. Note the test oscilloscope trace deflection away from the graticule centerline. Then adjust the Type 3S1 R832 so the trace rests at the centerline. The +12.2-Volt supply is now adjusted correctly.

c. Set the Type W Millivolts/Cm switch to 1. The test oscilloscope deflection factor is now 10 mV/Cm. Any 120 Hz ripple signal on the +12.2-Volt supply should not exceed 0.2 major divisions. There may be other noises visible, but observe only the 120 Hz content for this check. Return the Type W A Input Coupling to GND and the Vc Range to 0.

2. Check Type 3S1 +100-Volt Supply

a. Move the 1 X probe tip to TP817 (Fig. 8-4 insert). Set the Type W Comparison voltage to 10, Outer Dial to 1, Variable Dial to 0.00, the Millivolts/Cm switch to 20 and the Input Atten switch to 100. Recheck the DC Bal and Position control settings for a graticule centered zero volt trace. The test oscilloscope deflection factor is now 2 volts/cm with the graticule centerline representing +100 volts. 5% of 100 volts is 2.5 major CRT divisions.

b. Change the Type W A Input Coupling to DC and the Vc Range switch to +11, both at the same time. Check that the CRT trace does not move more than ±.2.5 major divisions from the graticule centerline. (The Type 3S1 +100 volts is more dependent upon the indicator oscilloscope +125 volts than upon the internal +12.2 volts. Variations will occur with different indicators.) Change the Type W A Input Coupling switch to AC and the Vc Range switch back to 0.

c. With the 1 X probe still connected to TP817, set the Type W Input Atten switch to 10 and the Millivolts/Cm switch to 1. The test oscilloscope deflection factor is now 10 mV/Cm, AC coupled. The 120 Hz ripple content must be no greater than 1 major CRT division peak to peak. Record the value in the Calibration Record and Index.

d. Disconnect the 1 X Probe from TP817 and return the Type W A Input Coupling to GND.

e. Disconnect the 1X probe from Type 3S1 and the Type W unit.

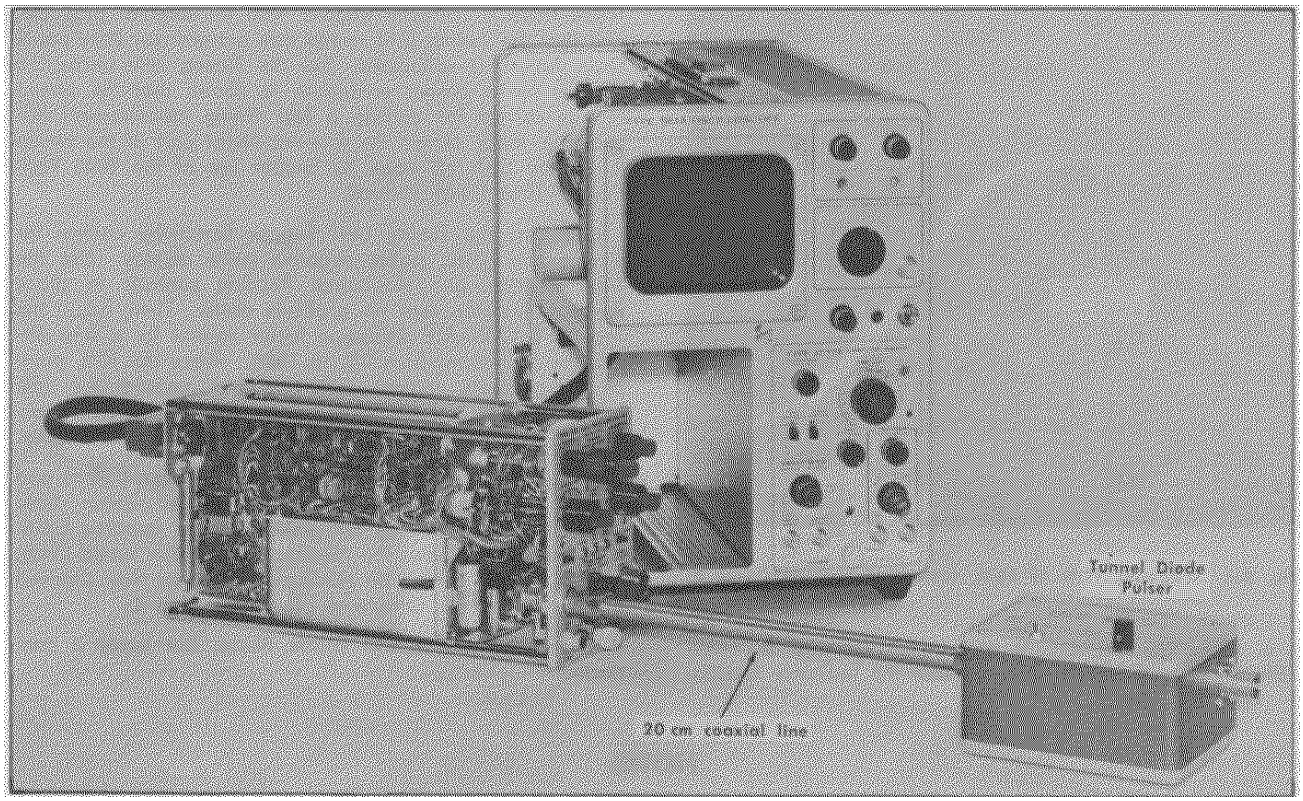

Fig. 8-5. Test equipment setup for Steps 3, 5, 6 and 7.

Control Settings

Type 3S1	
Display Mode Switch	CHAN A
SMOOTH-NORMAL	NORMAL
INTERNAL TRIGGER	**A**
HORIZ PLUG-IN	SAMPLING 3T-SERIES
Channel A	
A POSITION	Midrange
DC OFFSET	Midrange (5 turns from either end)
mVOLTS/DIV	100
VARIABLE	**Adjust for display similar to Fig. 8-6**
INVERT-NORM	NORM
Channel B	
B POSITION	Midrange
DC OFFSET	Midrange (5 turns from either end)
Type 3T77A	
Horizontal Position	Midrange
Time/Div	**1 ns**
Variable	Calib detent position
Time Expander	X10
Dots/Div	100
Time Position	**For display similar to Fig. 8-6**
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	**For triggered display**
Triggering Source	- Int
Recovery Time	Fully Counterclockwise
Tunnel Diode Pulser	
Power	On
Drive	Adjusted for clean negative step output signal

Connections

Use the GR 874-L20 20-cm air line between the Tunnel Diode Pulser Pulse Output connector and the Type 3S1 A INPUT connector.

3. Check Channel A 10% to 90% Risetime

NOTE

This step may be bypassed if the Type 3S1 has received maintenance and parts replacement that affect the Gate Generator or Sampler Bridge circuit. If no maintenance has been performed, then perform this step as a preliminary to steps 4, 5 and 6.

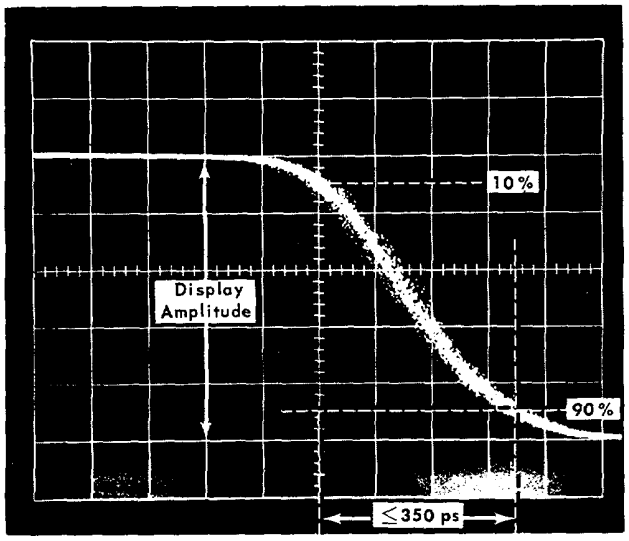

Fig. 8-6. 0.35 nSec 10% to 90% risetime of Type 3S1, Step 3.

a. Make the connections and control settings as listed following Fig. 8-5. Make certain that the Indicator Oscilloscope trace is correctly aligned with the internal graticule, and that the Timing Unit sweep rate (screwdriver front-panel Gain Adjust) is calibrated. See the Timing Unit instruction manual for a proper procedure to assure that the sweep rate is correct for making a fast timing measurement (for example, make certain the first non-linear part of the sweep is off the CRT left edge by proper use of the Time Position or Time Delay control).

b. Adjust the Timing Unit Trigger Sensitivity control for a minimum noise, stable negative pulse display. Use the Time Position and Horizontal Position controls to place the negative step near the graticule center. Then, adjust the Type 3S1 VARIABLE deflection factor control for a step display of 5 divisions from 0% to 100%. Place the 10% point at the graticule vertical centerline, and measure the time between there and the 90% point. Use Fig. 8-6 as an example of a correct 0.35 ns 10% to 90% risetime display.

c. Risetime of the Type 3S1 must be between 0.33 ns and 0.35 ns. If instrument risetime does not fall within these limits, the Type 3S1 may not make transient response limits. If part b above shows the risetime to be within stated limits, steps 4, 5 and 6 may be eliminated and you may proceed directly to step 7. Otherwise proceed to step 4.

d. Turn off the Tunnel Diode Pulser, but leave it connected.

NOTES

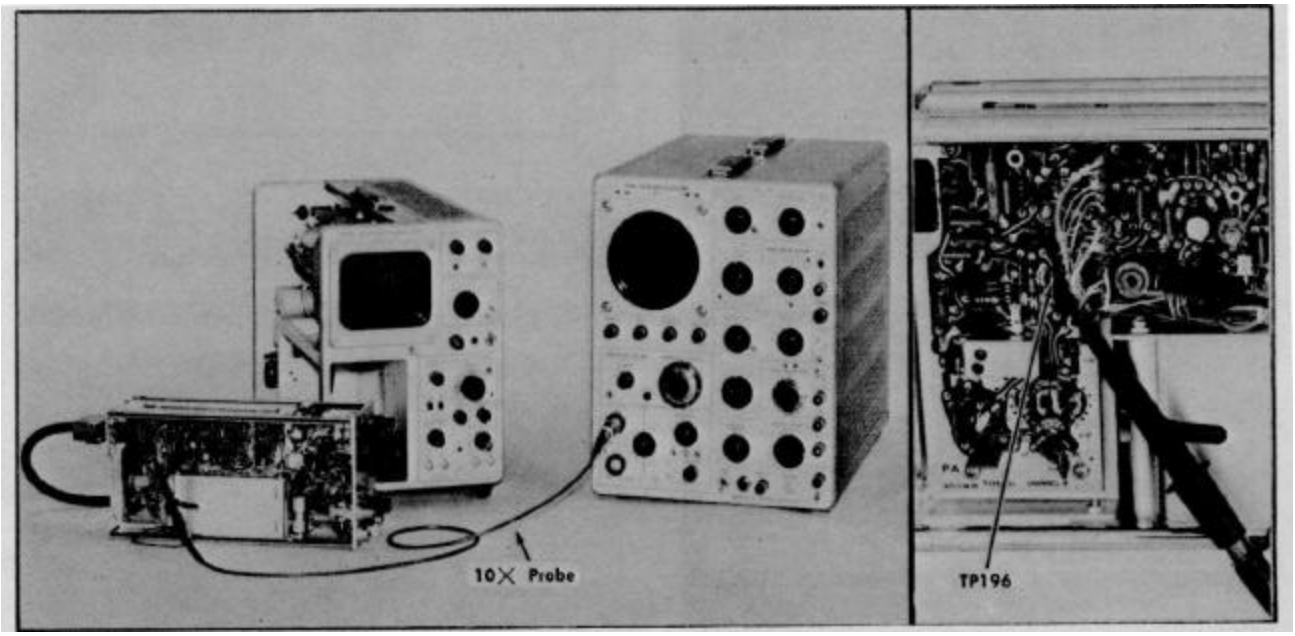

Fig. 8-7. Test setup for Step 4.

Control Settings

Type 3S1	
Display Mode Switch	CHAN A
SMOOTH-NORMAL	NORMAL
INTERNAL TRIGGER	A
HORIZ PLUG-IN	SAMPLING 3T-SERIES
Channel A	
A POSITION	Midrange
DC OFFSET	**Zero volts at A OFFSET OUT jack**
mVOLTS/DIV	100
VARIABLE	**CAL**
INVERT-NORM	NORM
Channel B	
B POSITION	Midrange
DC OFFSET	**Zero volts at B OFFSET OUT jack**
mVOLTS/DIV	100
VARIABLE	CAL
INVERT-NORM	NORM
Type 3T77A	
Horizontal Position	Midrange
Time/Div	**Optional**
Variable	Calib detent position
Time Expander	X1
Dots/Div	100
Time Position	Optional
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	**Fully Clockwise**
Triggering Source	-Int
Recovery Time	Fully Counterclockwise
Test Oscilloscope	
Sweep Rate	1 ms/Div
Triggering	+Line
Type W	
Vc Range	0
Comparison Voltage	**Optional**
Outer Dial	
Variable Dial	
A Input Coupling	**DC**
Input Atten	10
Display	A-Vc
Millivolts/Cm	**10**
Variable	Calib detent position
Position	Adjust in step 4

Connections

Connect the 10X probe to the A input connector of the Type W, and attach the probe ground clip to an outer conductor of one of the Type 3S1 front panel GR input connectors. There is no signal input during step 4.

4. Adjust Channel A Bridge Volts, R198

a. Make the connections and control settings listed under Fig. 8-7. The test oscilloscope deflection factor is 1 volt/cm.

b. Touch the 10X Probe tip to the A OFFSET OUT jack and carefully adjust the A DC OFFSET control for zero volts as observed on the test oscilloscope CRT. Repeat for Channel B.

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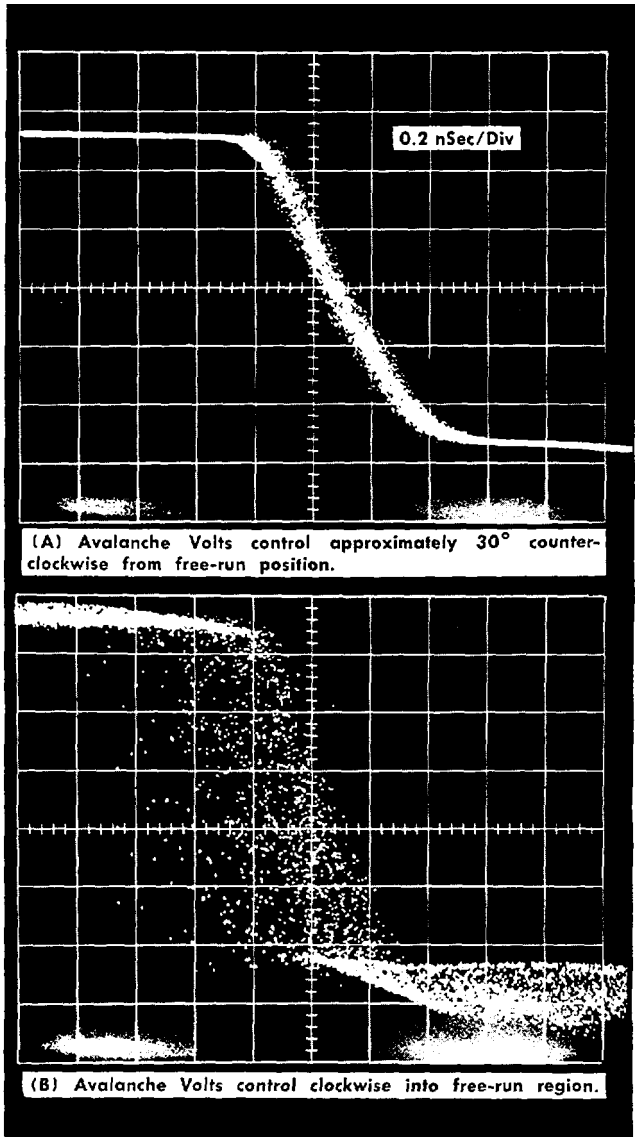

Fig. 8-8. (A) Correct; B) incorrect Avalanche Volts (RS) adjustments.

c. Move the 10X Probe ground clip to a convenient point near TP196, as shown in Fig. 8-7. Attach the probe tip to TP196. The test oscilloscope trace will move upward from its zero signal position. Use the Type W Position control and place the trace two major divisions above the graticule centerline.

d. Move the 10X Probe tip to TP199. If the BRIDGE VOLTS control is properly adjusted, the trace will move four major divisions down from the position set when measuring the voltage at TP196.

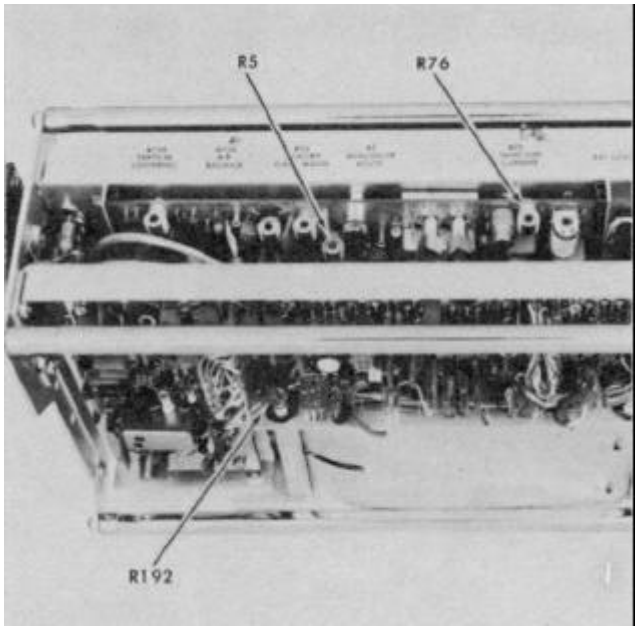

Fig. 8-9. Locations of Avalanche Volts (RS, Snap Off Current (R76) and Channel A Bridge Balance (R192) controls.

If the voltage difference between TP196 and TP199 is other than 4.0 volts, adjust the A Bridge Volts control, R198 (located just below the two test points), until the difference is 4.0 volts.

5. Adjust Avalanche Volts Control R5 (On Center Board)

Incorrect Avalanche Volts control adjustment is very obvious through the whole CRT display. Both a correct and an incorrect adjustment are shown in Fig. 8-8. The two displays were caused by approximately 30° difference in setting of the control.

a. Use the Tunnel Diode Pulser connected in step 3 (Fig. 8-5). Set the Type 3S1 deflection factor to 100 mV/div, and the Timing Unit for 0.2 nS/div sweep rate.

b. With a small blade screwdriver, adjust the Avalanche Volts control, R5 shown in Fig. 8-9 and located on the Center Board, a few degrees clockwise until the display breaks up as shown in Fig. 8-8. Now back the control a few degrees counterclockwise past the point where the display noise disappears.

The very noisy display is caused by self-oscillation of the Avalanche transistor, Q7. If the Avalanche Volts control is adjusted almost to oscillation, the instrument might become unstable during normal operation. This can be prevented by backing the control at least 5° into the stable region away from oscillation.

c. Turn off the Tunnel Diode Pulser, but leave it connected to Channel A for step 7.

6. Adjust Both Channel Bridge Bal Controls: Chan A, R192; Chan B, R492, and Adjust Snap Off Current Control, R76

NOTE

This step involves interacting adjustments of the Avalanche Volts control RS, and the Snap Off Current control R76, as well as the physical limits of the adjustment range of the two Bridge Bal controls, R192 and R492.

If the bridge diodes of a channel have been replaced during maintenance, the two pair conduction conditions affect this step. (See step 8 for diode replacement conditions.) If, using the procedure below, it is impossible to obtain proper Bridge Bal control adjustment, exchange D137C with D137D (in Channel B, D437C with D437D). Repeat the step. If balance is even more difficult, reverse D137C and D137D again. Now reverse D137A and D137B positions. Repeat the step. By this type of diode position exchange, the Balance controls can be made to operate properly. (Do not exchange diodes between channels, or between the front and rear pairs on one channel.)

a. Having adjusted the Avalanche Volts as in step 5, free run the Timing Unit. Carefully adjust both the A DC OFFSET and B DC OFFSET controls to deliver zero volts to the two OFFSET OUT jacks. Use the Type W in the test oscilloscope. Set both mVOLTS/DIV controls to 200.

b. Still displaying Channel A, use the A POSITION control to set the free run trace to the graticule centerline. Change the A mVOLTS/DIV switch to 100, and then to 50 if the trace doesn't move off screen. In either the 100 or the 50 position, adjust the A Bridge Bal control, R192 (location shown in Fig. 8-9) to return the trace to the graticule centerline. It is possible that the control will not have enough range, so leave it at its end of adjustment in the direction that brings the trace closest to the graticule centerline.

c. Adjust the Avalanche Volts control, R5, to move the free run trace just past the graticule centerline. Advance the A mVOLTS/DIV switch, one step at a time from 50 to 20 to 5, and adjust the A Bridge Bal control so the trace stays at the same vertical position for all positions of the mVOLTS/DIV switch.

d. Set the Display Mode switch to CHAN B. Use the B POSITION control and set the free run trace to the graticule centerline Change the B mVOLTS/DIV switch to 100, and then to 50 if the trace doesn't move off screen.

e. In either the 100 or 50 position, adjust the B Bridge Bal control, R492 (location shown in Fig. 8-10) to return the trace to the graticule centerline. As with Channel A, the B Bridge Bal control may reach the end of its adjustment range before it is properly set.

f. Set the B Bridge Bal control at the end of its range closest to a correct adjustment, and again adjust the Avalanche Volts control counterclockwise until the trace goes slightly past the graticule centerline.

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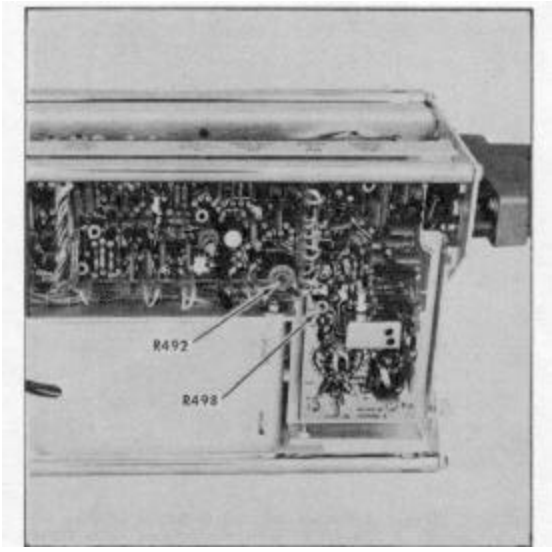

Fig. 8-10. Location of Channel B adjustment controls.

g. Advance the B mVOLTS/DIV switch, one step at a time from 50 to 20 to 5, and adjust the B Bridge Bal control so the trace stays at the same vertical position for all positions of the B mVOLTS/DIV switch.

h. Set the Display Mode switch back to CHAN A and readjust the A Bridge Bal control for no trace shift through the range of the A mVOLTS/DIV switch.

NOTE

During the second adjustment of the Avalanche Volts control in this step, observe the horizontal portions of the display for changes in noise content. Do not leave the control at a point where the noise is obvious, but rather where it is obvious that the noise is at a minimum. Then complete the Bridge Bal adjustments for both channels.

i. Set the Type 3S1 Display Mode switch to CHAN A.

j. Turn the Tunnel Diode Pulser back on and adjust the Timing Unit Trigger Sensitivity control for a stable negative step display. (It may be necessary to adjust the Time Position control to place the negative step in full view.)

k. Set the Timing Unit for 0.1 ns/div sweep rate and measure the negative step 10% to 90% risetime as in Fig. 8-11. If f the risetime is other than 0.35 ns, adjust the Snap Off Current control (R75 in Fig. 8-9). Clockwise rotation increases the time between the 10% and 90% points, and also reduces transient response aberrations. Counterclockwise rotation reduces the time between the 10% and 90% points, and increases the transient response aberrations. Set the control for a risetime of 0.35 ns as shown in Fig. 8-11.

l. Repeat the checks of both channel Bridge Bal controls with a free run no signal trace, but do not adjust the Avalanche Volts control unless absolutely necessary. If the Avalanche Volts control must be readjusted, repeat all of step 6 twice.

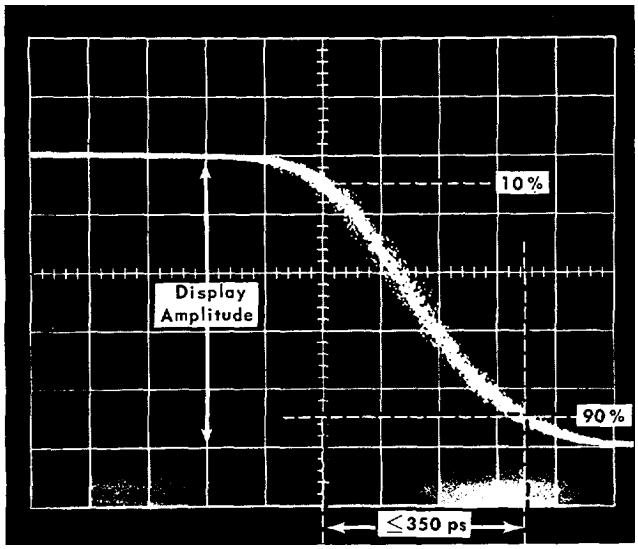

Fig. 8-11. Channel A Risetime, adjusted to 0.35 ns by Snap Off Current control, or Channel B risetime as adjusted by B Bridge Volts control.

7. Adjust Channel B Risetime Using B Bridge Volts Control, R498

a. Connect the Tunnel Diode Pulser to the B INPUT connector. Turn it on and set the Type 3S1 controls INTERNAL TRIGGER to B, Display Mode switch to CHAN B, B mVOLTS/DIV switch to 100. Adjust the Timing Unit for a stable triggered negative step display.

b. Check the displayed pulse 10% to 90% risetime. If it is other than 0.35 ns, adjust the B Bridge Volts control R498, shown in Fig. 8-10, for a display similar to that of Fig. 8-11. It is permissible to adjust R498 at any position throughout its range, including leaving it at either end. Clockwise rotation decreases the time between the 10% and 90% points and counterclockwise rotation increases the time between the 10% and 90% points.

c. If the B Bridge Volts control is adjusted, turn off the Tunnel Diode Pulser, free run the Timing Unit set the B DC OFFSET for zero volts, and readjust the B Bridge Bal control.

NOTES

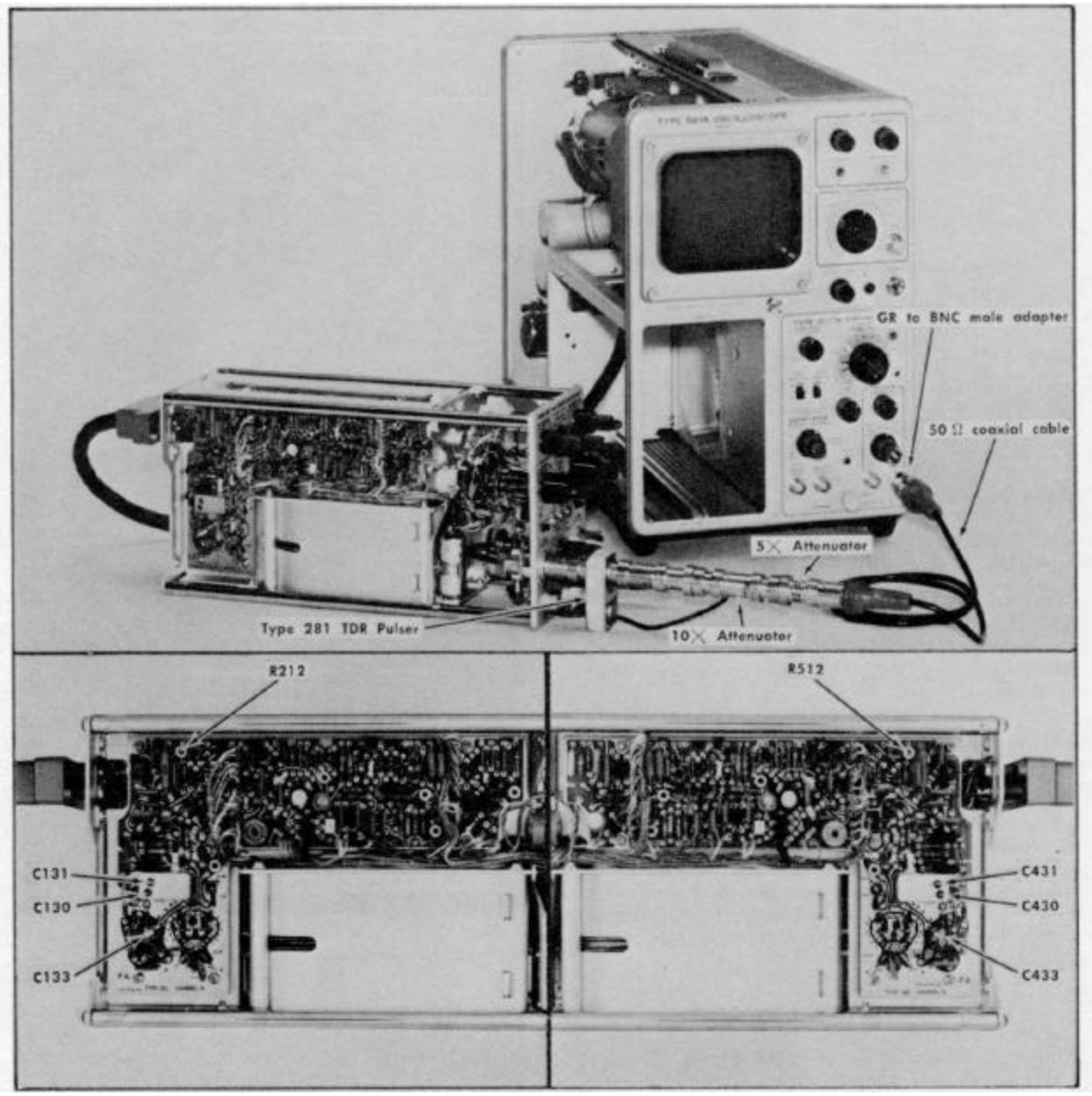

Fig. 8-12. Test setup and Blow-By adjustment locations, Step 8.

Control Settings

Type 3S1	
Display Mode Switch	CHAN A
SMOOTH-NORMAL	NORMAL
INTERNAL TRIGGER	**OFF**
HORIZ PLUG-IN	SAMPLING 3T-SERIES
Channel A	
A POSITION	Midrange
DC OFFSET	**As needed**
mVOLTS/DIV	**100**
VARIABLE	**5 Div display**
INVERT-NORM	NORM
Channel B	
B POSITION	Midrange
DC OFFSET	**As needed**
mVOLTS/DIV	**100**
VARIABLE	CAL
INVERT-NORM	NORM

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Type 3T77A	
Horizontal Position	Midrange
Time/Div	**2 ■Sec**
Variable	Calib detent position
Time Expander	X 1
Dots/Div	100
Time Position	**Centered negative step, see Fig. 8-13A**
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Ext Atten	
Trigger Sensitivity	**Triggered display**
Triggering Source	**+ Ext**
Recovery Time	Fully counterclockwise

Connections

Install the Type 281 TDR Pulser on the A INPUT connector and connect its power cord to one of the PROBE connectors. Connect the Type 281 other connector to the Timing Unit external trigger input connector with a 10X and a 5X 50 Ω attenuator in series, a 50 Ω coaxial cable and a GR to BNC adapter. See Fig. 8-12.

8. Check and Adjust Both Channel Blow-By Compensations: Chan A, C130-C131-C133; Chan B, C430-C431-C433

a. Make the connections and preliminary adjustments listed following Fig. 8-12, and obtain a waveform display similar to Fig. 8-13A.

b. Set the A mVOLTS/DIV switch to 10, and use the A DC OFFSET control to position the negative step to the CRT center. See Fig. 8-13B. Setting the mVOLTS/DIV control to 10 enlarges the display so that each CRT major division is 1% of the original amplitude shown in Fig. 8-13A.

c. Check the displayed waveform deviation from a straight line. The instrument is within proper blow-by adjustment limits if the display positive and negative peaks fall within two major graticule divisions (±1%). If the peak-to-peak display is greater than 2 major divisions, adjustment of the blow-by capacitors is required.

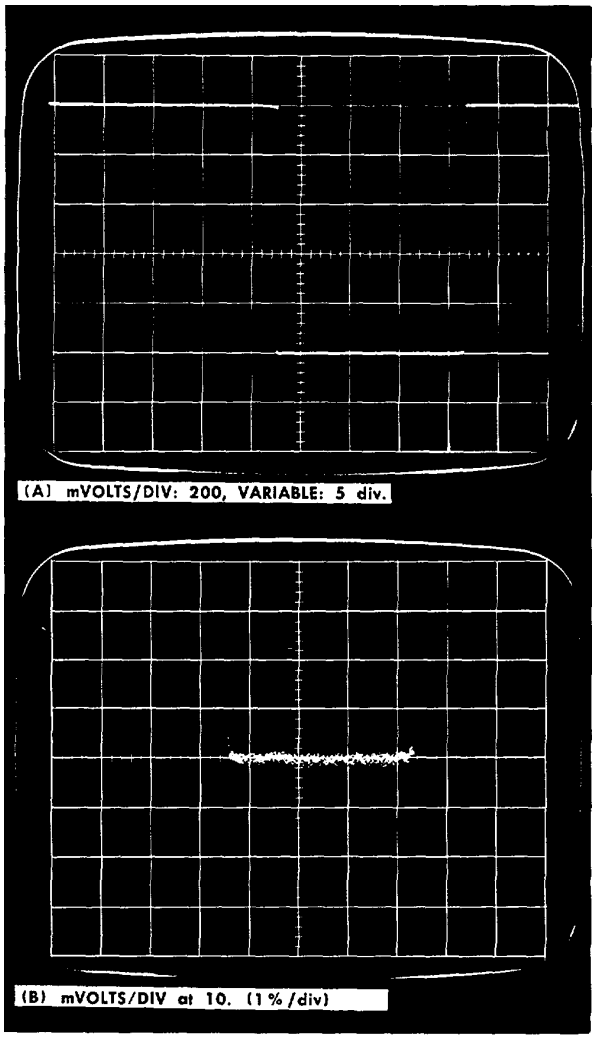

Fig. 8-13. Preliminary setup waveforms for Step 8.

NOTE

In the adjustment sequence to follow, C133 has the most obvious effect upon the display. This is because its time constant is considerably longer than that of C130 or C131. C131 effect is seen in the first 1.5 to 2 s of the display. C130 effect is very slight, seen in the first 0.5 to 1 ■s of the display. Fig. 8-14 shows the effect of each capacitor upon the display. Study it before making any adjustments. It is recommended that adjustments be made to the longer time constant capacitor (C133) first (if the display indicates that need), and then to C131 and C130 in that order. C130 and C131 typically adjust correctly when the screw heads are about 1/16 inch to 3/32 inch from the cover plate. C130 typically adjusts correctly at about 1/2 capacitance.

c. Adjust C133 for the best overall flatness of the display. Use an insulated, small screwdriver-bit tool (item 21 of Equipment Required) to make the adjustment. Remove the tool after each adjustment and if necessary, adjust the DC OFFSET control to return the display to the CRT. It is recommended that the final adjustment be not over 1/4 to 1/2 turn, and then check the display.

d. After assuring that C133 is properly adjusted, use the adjusting tool and adjust C131. Try 2 or 3 turns the first time, then remove the tool and observe the display change. The adjusting tool makes the display very noisy while in contact with the adjusting screw. Remove the tool to observe the adjustment effect.

C131 affects both the leading and trailing edges of the display, as shown in Fig. 8-14B.

e. Change the Timing Unit Dots Per Divisions control to 10 and check that the feedback loop gain is adjusted to unity. If the first dot is considerably above or below the leveled display, set the front panel A or B DOT RESPONSE control to midrange. Then adjust the internal Loop Gain

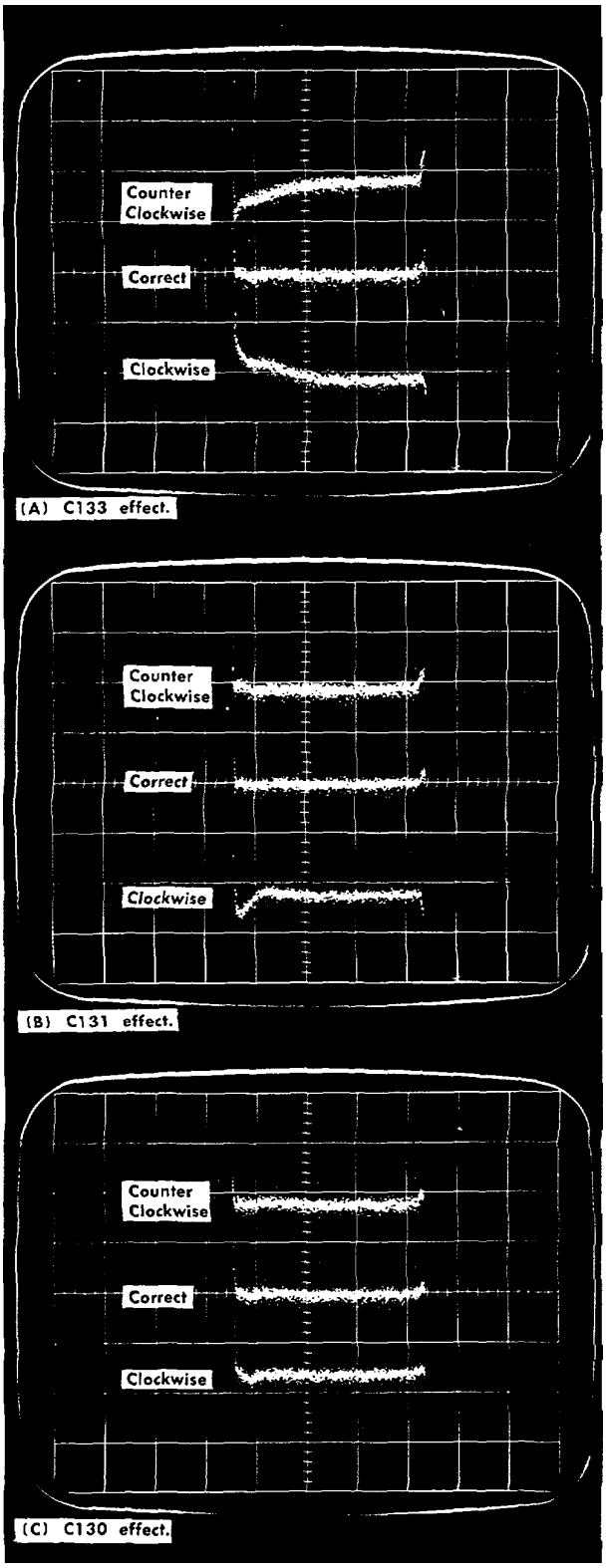

Fig. 8-14. Blow-By adjustments, Step 8. Sweep Rate: 2 msec/div. Vertical: 1% per div.

control, R212 (or R512 in Channel B) shown in Fig. 8-12, until the first dot is level with the rest of the display. Return the Timing Unit Dots Per Division control to 100.

f. Adjust C130 several turns at a time, and carefully note the effect upon the display leading edge. The capacitor will probably adjust with the screw closer to the shield than is C131.

Repeat the adjustment of all three capacitors if the display is not flat. Repeat the whole step for Channel B.

NOTE

If the display flatness cannot be adjusted within one major division (1% total), then the sampling bridge diodes are probably at fault. As a check, and only if one channel can be properly adjusted, diodes from the good channel can be substituted into the channel that does not adjust.

Sampling Bridge Diode Substitution Conditions

If it is decided to substitute either new diodes, or diodes from a properly adjusted channel into an incorrectly functioning channel, several precautions must be followed.

1. Diodes must not be touched by the hands. Use a small plastic diode handling tool, Tektronix Part No. 006-0765-00 (a plastic handling tool is shipped with each set of new diodes). If the diodes are handled by the hands, they must be cleaned with soft dry tissue before installation.

2. Diodes ore installed in two color coded pairs. One color code is used on the two input diodes, and another color code is used on the two output diodes (output to the Pre-Amp input). Observe the colors, and be certain each pair is used in its proper location. (If the colors of new diodes differ from those in the instrument, the new diodes are packed with correct color coding information so they can be correctly installed.

3. The color coding dots are located at the cathode end of the diodes. All diodes are installed with the cathode ends away from C133 (and C433 in Channel B). The input pair are toward the instrument bottom, and the output pair are toward the instrument top, in both channels.

4. When substituting diodes between channels, turn the indicator oscilloscope power off. Do not turn the power back on until all diodes are in place in both channels.

5. After changing diodes, repeat the Calibration Procedure, beginning with step 5.

9. Check Transient Response

This step checks the individual channel transient response at three sweep rates, and should not be performed unless step 8 adjustments produce satisfactory transient response limits for the 2 ms/div display.

a. Use the equipment connections and 1%/div display of step 8. If step 8 concluded with the Type 281 installed on Channel B, start this step on Channel B.

b. Set the Timing Unit sweep rate at 0.2 ms/div and obtain a stable display internally triggered on the - slope. Horizontally position the display so the negative step starts at the graticule

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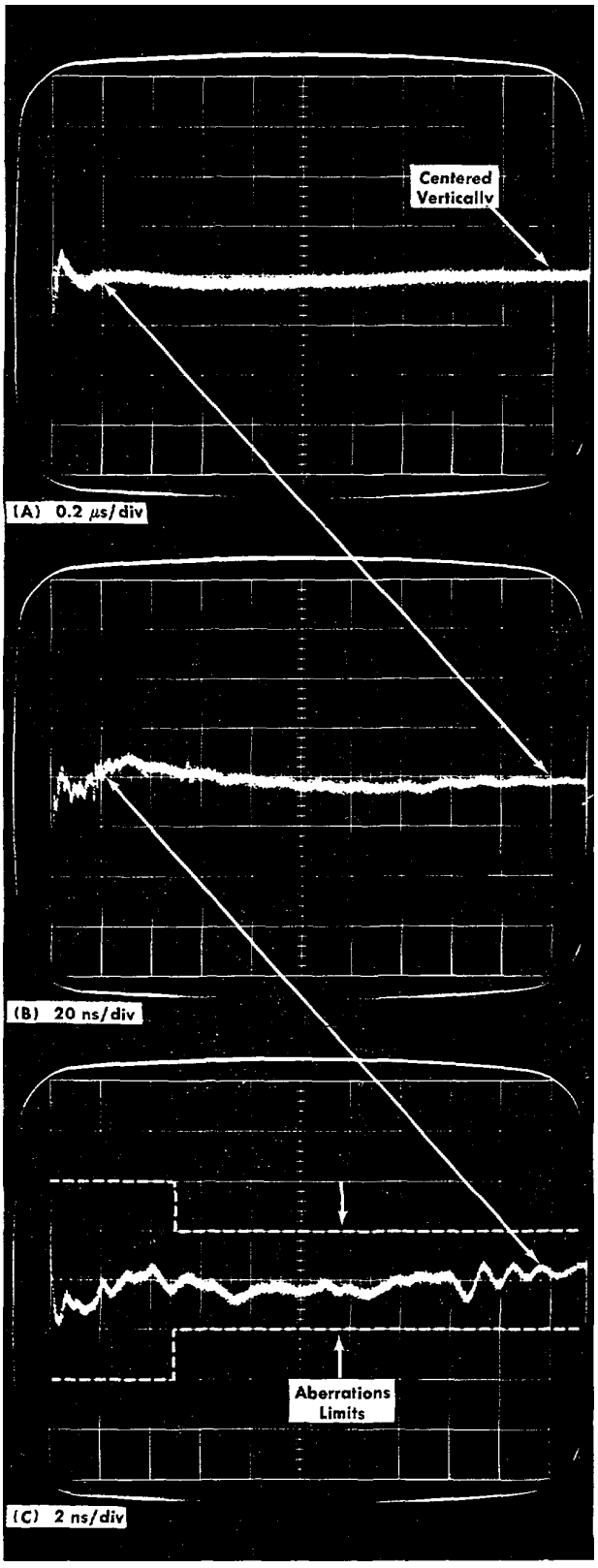

Fig. 8-15. Check of transient response. Step 9.

left edge. Vertically position the display so the trace passes through the graticule centerline as it passes off the graticule at the right. See Fig. 8-15A. Check that the total display (after the negative step) lies within ±1 major division of the graticule centerline.

c. Note the vertical position of the waveform one major division in from the graticule left edge. Fig. 8-15A shows an example with the trace about 0.1 major division below the graticule centerline.

d. Change the sweep rate to 20 ns/div and horizontally time position the display (with the Time Position control) as in Fig. 8-15B. Vertically position the right end of the trace to the graticule reference as was noted one division in from the left edge at 0.2 ms/div. Fig. 8-15 arrows show the vertical alignment points. Check that the total display lies within ±1 major division of the graticule centerline.

e. Note the vertical position of the waveform one major division from the graticule left edge.

f. Change the sweep rate to 2 ns/div and horizontally time position the display as in Fig. 8-15C. Vertically position the right end of the trace to the graticule reference as was noted one division in from the left edge at 20 ns/div. Check that the total display lies within the marked aberration limits of Fig. 8-15C.

The procedure just completed maintains the same vertical reference stated in 0.2 ms/div (b above). The reason for the three separate sweep rates is that the sampling process does not have adequate fast resolution at low sweep rates, and by looking at the display three times, full resolution is obtained and observed.

g. Repeat the procedure for the other channel, changing both the INTERNAL TRIGGER and the Display Mode switches

h. Leave the Type 281 TDR Pulser attached for step 10.

10. Adjust Memory Gate Width Control, R52 ◐

a. Set the Timing Unit sweep rate to 2 ms/div, the Dots Per Div switch to 10 and trigger internally on the minus slope. Place the Type 281 on the Type 3S1 A INPUT connector and obtain a display similar to Fig. 8-16A.

The test oscilloscope may be required if R52 does not adjust correctly as described in (b) below.

b. Adjust the Memory Gate Width control, R52 shown in Fig. 8-17, for maximum feedback loop gain.

Maximum feedback loop gain is attained when the first dot after a step transition is the farthest from the last dot just before the step transition occurs. This adjustment may not produce unity feedback loop gain, as is shown in Fig. 8-16B, but rather can produce less than (Fig. 8-16A), or more than (Fig. 8-16C) unity gain. It is important that the Memory Gate Width control be adjusted for maximum possible loop gain, regardless of whether unity gain is attained or not.

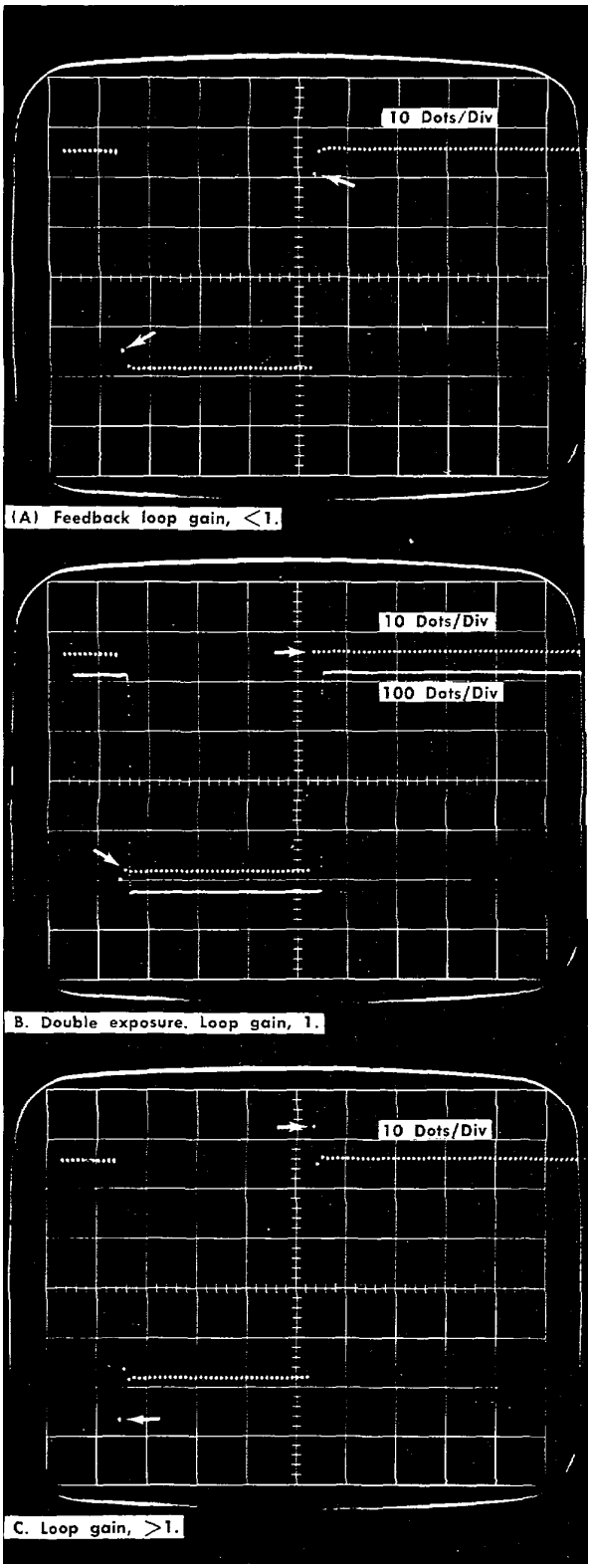

Fig. 8-16. Dot response waveforms for Step 11.

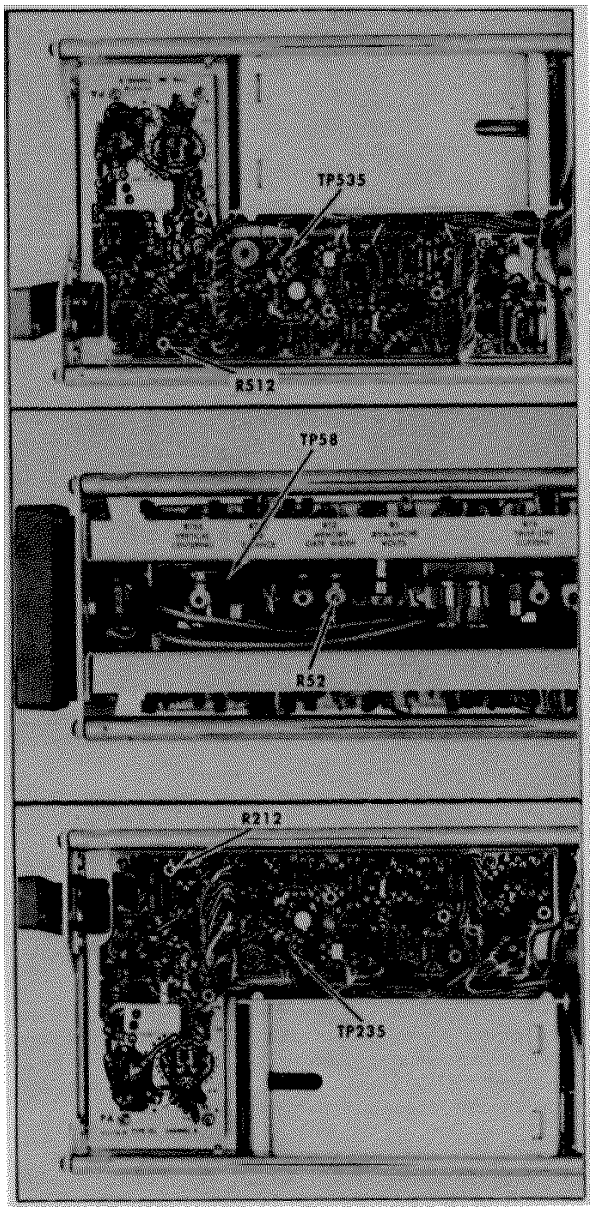

Fig. 8-17. Memory Gate Width control (R52) and test points of Step 10.

NOTE

If the Memory Gate Width control can be adjusted so that the displayed loop gain obviously passes through maximum, there is no need to do any more of this step. If R52 adjusts near its range limit, or if maintenance has been performed inside the loop, the rest of this step can be performed to assure proper operation of both channels.

c. To check the Memory Gate circuit output pulse, attach the test oscilloscope 10X Probe to TP58 (see Fig. 8-17).

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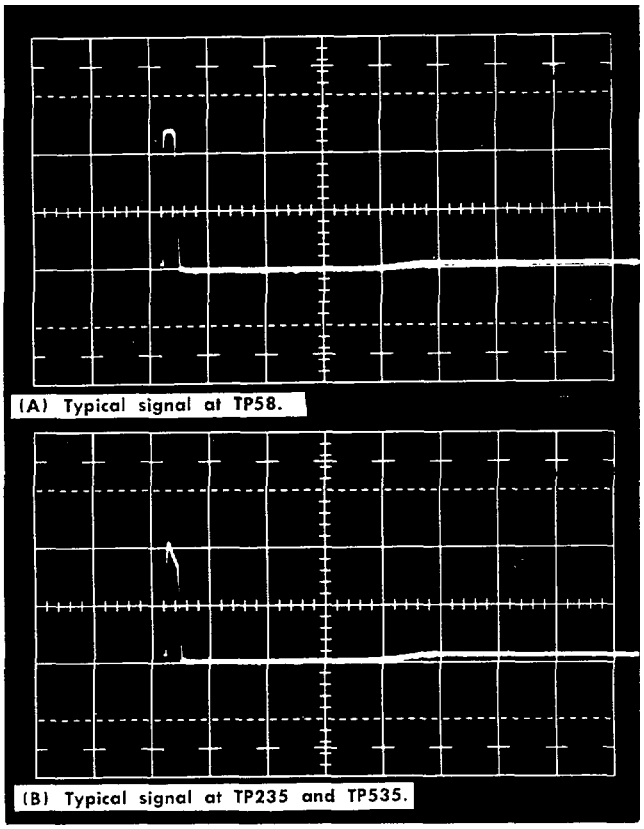

Fig. 8-18. Test oscilloscope waveforms of Memory Gate Width test point. (Sweep rate: 1 ms/div. Vertical: 5 V/div.

Use a 10X Probe on the test oscilloscope, and set the controls for 5 volts/div at 1 ms/div, +Internally triggered. The test oscilloscope display should be similar to Fig. 8-18A. Fig. 8-18A shows that the signal at TP58 has a flat region at the top.

d. If one channel operates and the other does not, a check of the Memory Gate drive signal to each Memory circuit can be made at TP235 and TP535 shown in Fig. 8-17. The signal at TP235 and TP535 is not flat at the top, but rather should appear similar to Fig. 8-188.

11. Adjust Loop Gain: Chan A, R212: Chan B, R512

a. Use the Type 281 connected to Channel A as in step 10, with the Timing Unit still at 2 ms/div. Change the Timing Unit Dots Per Div switch to 100.

b. The display should be similar to Fig. 8-168 solid line of 100 dots/div. Note the corners at the end of both the positive and negative step transitions. Then go back to 10 dots per division.

c. Set the two front panel screwdriver adjust dot response controls to midrange. Then adjust the Channel A internal loop gain control, shown in Fig. 8-17, so the transition corners are as similar as possible to the corners at 100 dots per division. Check back and forth from 100 to 10 dots per division to be certain the display is correct.

d. Adjust the front panel A DOT RESPONSE control fully clockwise. The first dot at the top of the transition must be at least 1.05 times the step amplitude. (In the display shown in Fig. 8-16C, the main pulse is about 4.5 divisions; therefore, the first dot must now be at least 4.75 divisions from the pulse bottom,)

e. Adjust the A DOT RESPONSE control fully counterclockwise. The first dot at the top of the transition must be at least 0.95 times the step amplitude, or less. (In the display shown in Fig. 8-16A, the main pulse is about 4.5 divisions; therefore, the first dot must be at 4.26 divisions or less from the pulse bottom.)

f. Adjust the A DOT RESPONSE control so the display is the same at both 10 and 100 dots per division, as shown in Fig. 8-168.

g. Move the Type 281 to the Type 3S1 8 INPUT connector. Change the INTERNAL TRIGGER switch to 8, the Display Mode switch to CHAN B, and obtain a stable display

h. Check the display corners at the ends of both the positive and negative transitions at 100 dot per division. At 10 dots per division, adjust the Channel B internal Loop Gain control, R512 shown in Fig. 8-17, for correct dot response. Check back and forth between 100 and 10 dots per division to see that the display is correct (similar to Fig. 8-16B).

i. Repeat steps d, e, and f on Channel B.

12. Check Both Channels Dot Response When Smoothed

a. Use the setup for step 11. Change the Type 3S1 SMOOTH-NORMAL Switch to SMOOTH. Adjust the VARIABLE mvolts/div control until the maximum display amplitude is 5 divisions. The display should be similar to Fig. 8-19, with the first

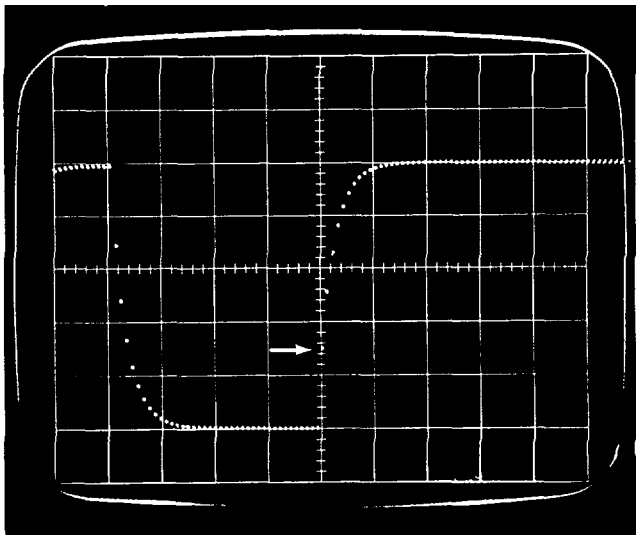

Fig. 8-19. Dot response Smoothed. Step 12.

dot of each transition not more than 1.5 divisions from the previous dot.

b. Repeat the same procedure for the other channel. Leave the setup for step 13.

13. Adjust Smoothing Balance Control: Chan A, R247; Chan B, R547

a. With or without a signal, but with a free run trace or a triggered display, change the Type 3S1 SMOOTH-NORMAL switch back and forth between its two positions There should be no vertical shift in the trace between the two switch positions

b. If the trace does shift vertically, note the trace position with the SMOOTH-NORMAL switch at NORMAL Change it to SMOOTH and adjust the Smoothing Balance control, R247 (or R547 of Channel B) shown in Fig. 8-20, to move the trace back to its position when the switch was at NORMAL Repeat this several times until there is no trace shift when the SMOOTH-NORMAL switch position is changed.

c. Repeat for the other channel.

14. Adjust Inverter Zero Controls: Chan A, R283; Chan B, R583

a. Remove the Type 281 from the Input connector. Free run the Timing Unit using 100 dots per division. Check that the DC OFFSET control both produce zero volts at the OFFSET OUT connectors. Place the Display Mode switch to CHAN A, both INVERT-NORM switches to INVERT and position the trace vertically to the graticule centerline. Set both VARIABLE mvolt/div controls to CAL.

b. Change the Chan A INVERT-NORM switch to NORM and adjust the Chan A Inverter Zero control, R283 shown in Fig. 8-20, until the trace is again at the graticule centerline. Change the INVERT-NORMAL switch between its two positions and check that the trace remains at the some vertical position

c. Repeat the above procedure for Chan B with the Display Mode switch at CHAN B, and adjust R583 shown in Fig. 8-20 in the same manner.

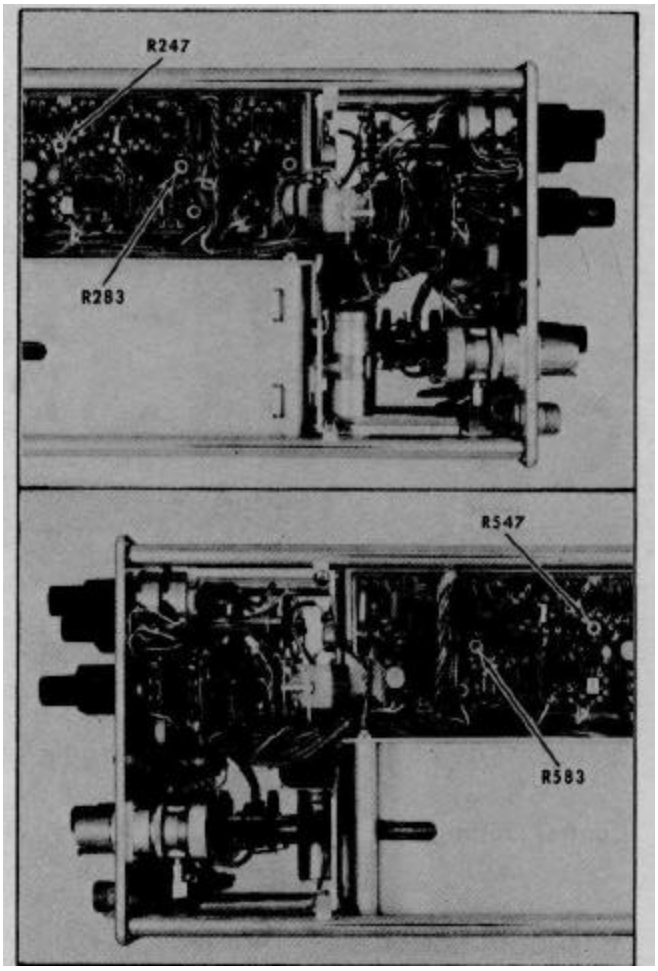

Fig. 8-20. Location of Smoothing Bal controls and Inverter Zero controls. Steps 13 and 14.

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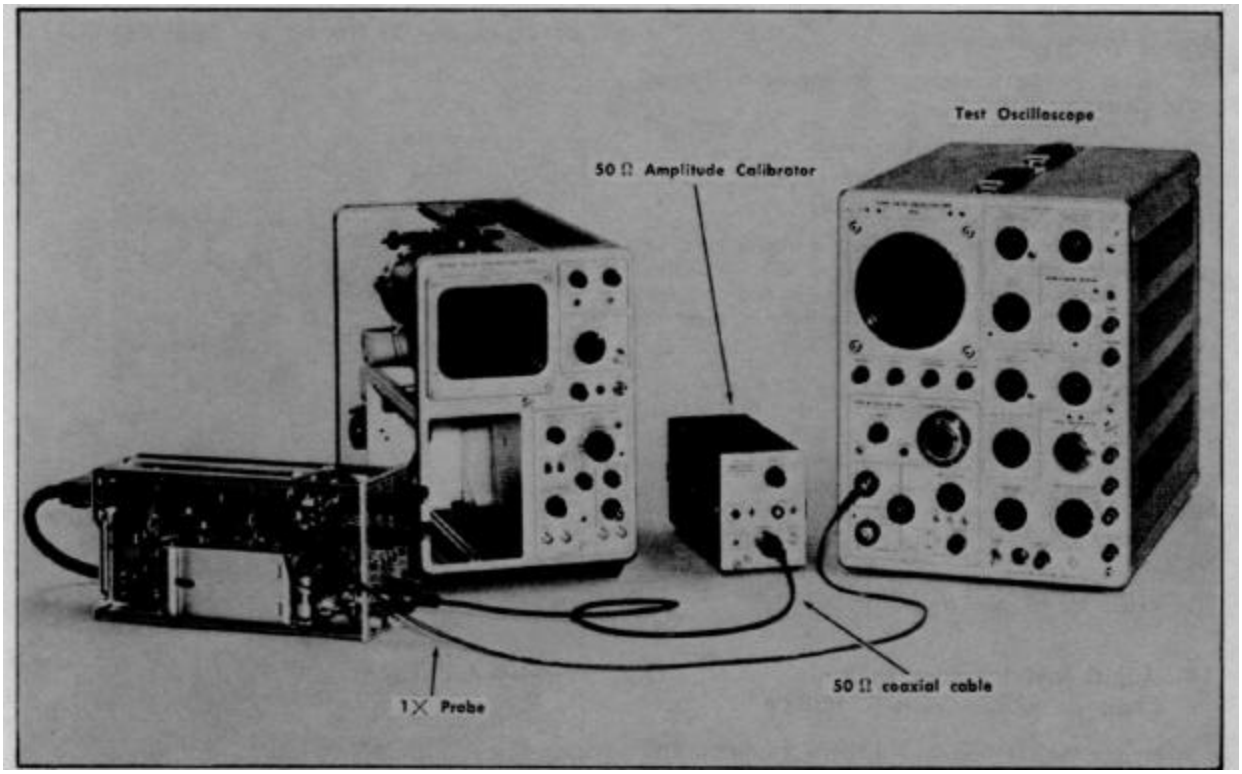

Fig. 8-21. Test setup for setting digital gain, Step 15.

Control Settings

Type 3S51

Display Mode Switch	**CHAN A**
SMOOTH-NORMAL	**NORMAL**
INTERNAL TRIGGER	A
HORIZ PLUG-IN	SAMPLING 3T-SERIES

Channel A

A POSITION	Midrange
DC OFFSET	Zero Volts Out
mVOLTS/DIV	200
VARIABLE	CAL
INVERT-NORM	NORM

Channel B

B POSITION	Midrange
DC OFFSET	Zero Volts Out
mVOLTS/DIV	200
VARIABLE	CAL
INVERT-NORM	NORM

Type 3T77A

Horizontal Position	Midrange
Time/Div	2 *m*Sec
Variable	Calib detent position
Time Expander	X 1
Dots/Div	100
Time Position	Optional
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Triggered Sensitivity	**Triggered display**
Triggering Source	+Int
Recovery Time	Fully counterclockwise

50 W Amplitude Calibrator

Volts Control	1.2
Output Signal	Square wave

Test Oscilloscope

(Use Type W Plug-In Unit or specially calibrate the vertical unit to better than 1% accuracy at 1 Volt/Div.)

Sweep Rate	l0 ms/div
Vc Range	0
Comparison Voltage	
Outer Dial	**0**
Variable Dial	**»6.5**
Input Atten	**10**
Display	A-Vc
Millivolts/Cm	**50**

Connections

Install the 1X Probe onto the Type W A Input connector. Connect the 50 Ω Amplitude Calibrator Output connector to the Type 3S1 A INPUT connector with a 50 Ω coaxial cable.

Connect the 1X Probe ground clip to the Type 3S1 frame near TP313, and connect the probe tip to TP313, as shown in Fig. 8-22.

15. Adjust Internal Digital Gain Controls: Chan A, R301; Chan B, R601

NOTE

The procedure shown here applies even when adjusting the Digital Gain controls while calibrating the Type 3S1 with a Type 567 or Type 568 indicator oscilloscope. By adjusting the digital gain controls in this manner, the instrument is within gain limits for use with all Type 6R1A or Type 230 Digital Units.

a. Make the connections and control settings listed under Fig. 8-21. Obtain a stable display on both the sampling system and the test oscilloscope.

b. Set the Type W Vc Range switch to +11 and use the Variable Comparison Voltage dial to set the test oscilloscope display bottom to the graticule centerline. Set the Type W Millivolts/Cm switch to 5 and position the display bottom to the graticule centerline. Read and record the measured voltage about 7 volts.

c. Set the Type W Comparison Voltage outer dial to 1, and turn the Variable dial counterclockwise until the test oscilloscope display top is at the graticule centerline. Read and record the measured voltage.

d. Subtract the two Comparison Voltage recorded values. The difference should be 6 volts. If it is other than 6 volts, adjust the Type 3S1 internal Digital Gain control, R301 shown in Fig. 8-22, until the two voltage readings are 6 volts different.

NOTE

The signal at both TP301 and TP601 is required to be within 3% when the INVERT-NORM switch is at NORM, for all positions of the mVOLTS/DIV switches. The 50 Ω Amplitude Calibrator Volts control provides the proper signal amplitudes so it and the mVOLTS/DIV controls track, and the Type W display will always be 1.2 volts, ±3%. If any switch position is outside its tolerance, a second adjustment of the Digital Gain control may bring all values within proper limits. When checking all positions of the mVOLTS/DIV controls, it will be necessary to externally trigger the sampling Timing Unit from the 50 Ω Amplitude Calibrator Trigger Output connector. The accuracy of the signal at both TP301 and TP601 is required to be within 5% when the INVERT-NOM switch is at INVERT. Record the signal at all positions of the mVOLTS/DIV switch.

e. Repeat the step for Channel B; test point and adjustments are shown in Fig. 8-22.

f. Leave the equipment setup for step 16.

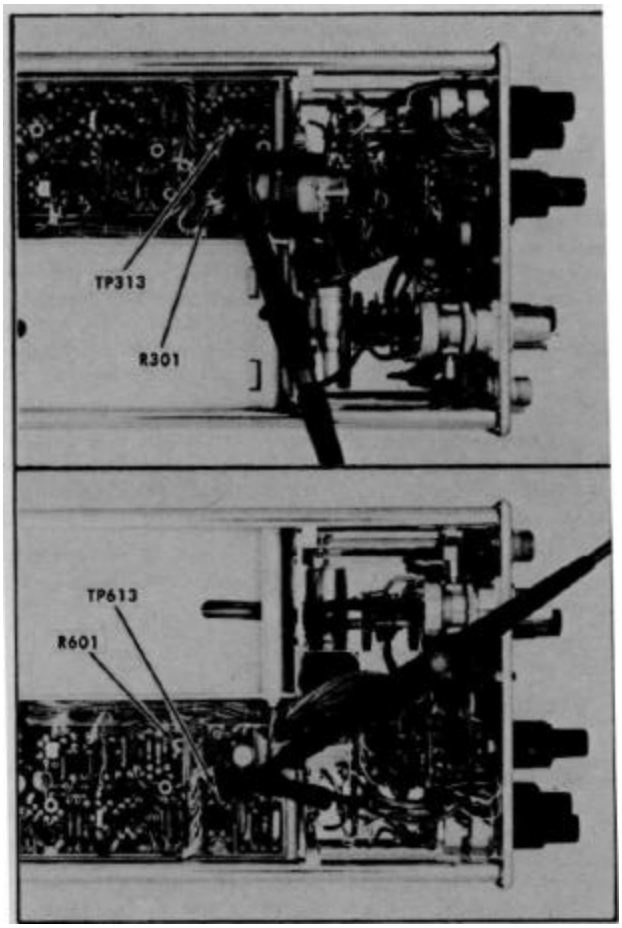

Fig. 8-22. Test points and adjustments for Step 15.

16. Check A OUT and B OUT Signals (AC Signal Only)

a. With the 50 Ω Amplitude Calibrator still connected to Channel B, move the test oscilloscope 1X Probe to the front panel B OUT connector.

b. Set the Type W controls:

Vc Range	0
Input Atten	**10**
Coupling	DC
Millivolts/Cm	50
Comparison Voltage	
Outer Dial	0
Variable Dial	**0**
Display	A-Vc

c. Set the 50 Ω Amplitude Calibrator Volts control to 1.2 and both Type 3S1 mVOLTS/DIV controls to 200.

The test oscilloscope display should be 2.4 divisions peak to peak, starting near zero and going negative.

d. Set the Type W Vc Range switch to -1.1 and the Millivolts/Cm switch to 5. Adjust the Comparison Voltage variable dial until the display top is at the graticule centerline. Read and record the comparison voltage.

Ⓑ

e. Set the Type W Comparison Voltage outer dial to 1, and adjust the Variable dial until the display bottom is at the graticule centerline. Read and record the comparison voltage.

f. Subtract the two comparison voltages to obtain the B OUT signal amplitude. It must be 1.2 volts +1% to -3%. The actual voltage must be within 2% of the input voltage (with the controls as set), but the Type W 1 MΩ input resistance loads the signal output 10 kΩ source impedance 1%. The A OUT and B OUT zero signal portion of the display (test oscilloscope display top) will probably not be at zero volts when the OFFSET OUT jack voltage is zero. This is normal. No limits are given for this condition, but the difference from zero will usually be only a fraction of a volt.

g. Change the Type 3S1 Display Mode switch to CHAN A. Move the 50 Ω Amplitude Calibrator signal cable to the A INPUT connector. Change the INTERNAL TRIGGER switch to A and obtain a stable display.

h. Move the test oscilloscope 1X Probe to the A OUT connector and repeat part (c) on Channel A. The same limits apply.

NOTE

The checks just completed test the feedback loop overall gain in accordance with Section 1 of this manual. The procedure does not call out or use the formula of Section 1, but the control settings take Section 1 into account so the test is valid. If the A OUT or B OUT signals are more than 3% low, use a good resistance bridge and check R298 and R299 in Channel A, or R498 and R599 in Channel B as a likely source of the error. (See the Maintenance section for parts location pictures.)

i. The 50 Ω Amplitude Calibrator and test oscilloscope are both used in step 17.

17. Check VERT GAIN Control Range and Set VERT GAIN, R764

a. Connect the 50 Ω Amplitude Calibrator to the Type 3S1 B INPUT connector. Set the calibrator Volts control to 1.2.

b. Set the Type 3S1 mVOLTS/DIV controls to 200, the VERT GAIN control fully counterclockwise and both VARIABLE controls to CAL. Set the INTERNAL TRIGGER switch to B and obtain a stable display at 2 *m*sec/div.

c. Set the test oscilloscope to operate with a 1X Probe, DC Coupled input, and a vertical deflection factor of 2 volts/div.

d. Set Type W controls:

Input Atten	**100**
Millivolts/Cm	**20**
Comparison Voltage	
Outer Dial	0
Variable Dial	**»8.0**
Vc Range	0

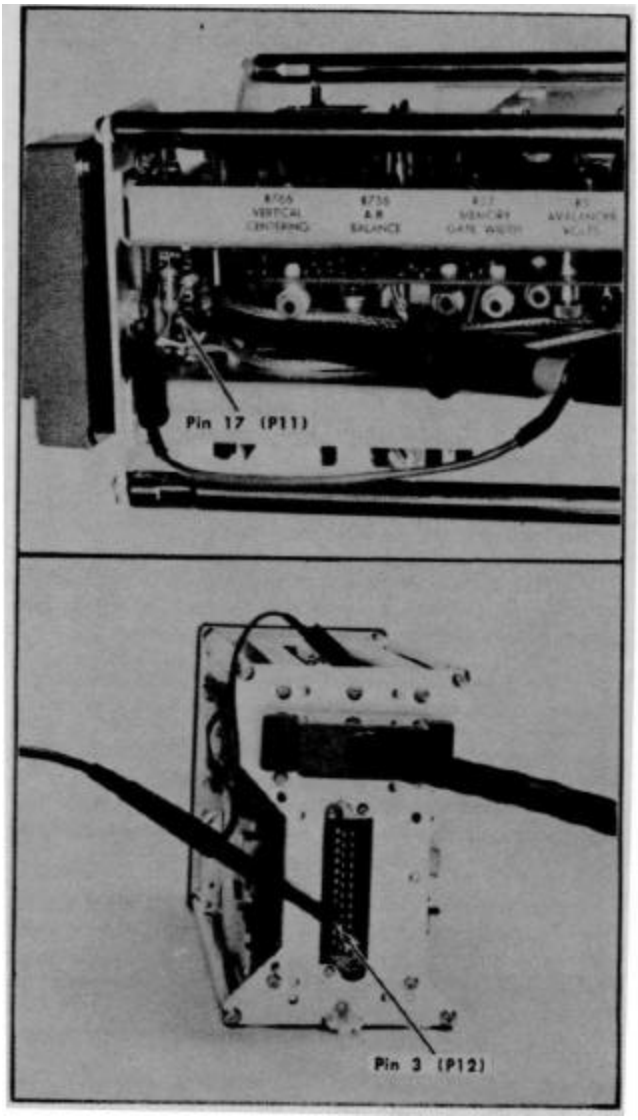

Fig. 8-23. Step 17 test points.

e. Connect the 1X Probe ground clip to the instrument back panel and touch the tip to Pin 3 of P12 (the vertically mounted interconnecting plug). See Fig. 8-23A for probe location.

f. Set the Type W Vc Range switch to +1.1, adjust the test oscilloscope triggering controls for a stable display at 10 ms/cm, and read the peak to peak amplitude of the test oscilloscope display. (DC coupling is used here to avoid the AC coupling differentiation of the signal, and the Type W Comparison Voltage as a display offset control to bring the signal into view.)

g. Record the signal voltage.

h. Change the Type W Input Atten switch to 1000, and the Comparison Voltage outer dial to 1 (deflection factor now 20 volts/div). Move the 1X Probe to measure the signal at Pin 17 of P11 (the horizontally mounted interconnecting plug). See Fig. 8-23B for probe location.

Ⓐ

i. With the Type W Vc Range switch at +1.1, measure and record the peak to peak display amplitude measured on the test oscilloscope.

j. Divide the larger number into the smaller number (of f) to obtain a gain figure. The gain must be equal to or less than 9. If the gain is greater than 9, either the VERT GAIN control resistance is low, or R777 resistance is high. (R777 is the Output Amplifier feedback resistor.)

k. Set the Type 3S1 VERT GAIN control fully clockwise and again measure the test oscilloscope display peak to peak voltage. Divide this voltage into the smaller number (of f) to obtain a gain figure. The gain must be equal to or greater than 13. If the gain is less than 13, either the VERT GAIN control still admits resistance in the circuit, or R777 is low in value.

l. Set the VERT GAIN control so the Type 3S1 indicator oscilloscope display is exactly 6 divisions peak to peak.

m. The test oscilloscope is not used in step 18. Set the Type W Vc Range switch to 0, and remove the probe from the Type 3S1.

18. Adjust A-B Bal Control, R756 (Channel A Vert Gain) ◐

a. Move the 50 Ω Amplitude Calibrator signal to the Type 3S1 A INPUT connector. Set the INTERNAL TRIGGER switch to A, and the Display Mode switch to CHAN A. Obtain a stable display.

b. Adjust the A-B Bal control, R756 shown in Fig. 8-24, for a display exactly 6 centimeters peak to peak on the indicator oscilloscope CRT.

c. Leave the equipment as connected.

19. Check mVolts/Div VARIABLE Control Range and UNCAL Lamps

a. Use the 50 Ω Amplitude Calibrator as connected to Channel A at the lost step (1.2-volt signal).

b. Turn the Channel A VARIABLE control fully counterclockwise and note the indicator oscilloscope display peak-to-peak amplitude. The display should be equal to or less than 0.7 times the CAL amplitude (6 div at CAL; ≤4.2 div with VARIABLE fully ccw).

c. Change the 50Ω Amplitude Calibrator Volts control to .6. Obtain a stable 3-division indicator oscilloscope display.

d. Turn the Channel A VARIABLE control fully clockwise and note the indicator oscilloscope display peak to peak amplitude. The display should be equal to or greater than 2.5 times the CAL amplitude (3 div at CAL; ≥7.5 div VARIABLE fully cw).

NOTE

Step 19 check is significant after maintenance and changing of a VARIABLE control. If the display amplitude cannot be reduced to 70% of the CAL display amplitude, the control resistance is low. If the display amplitude cannot be expanded 2.5 times the CAL amplitude, either there is resistance remaining in the control, or the Inverter Amplifier gain is low.

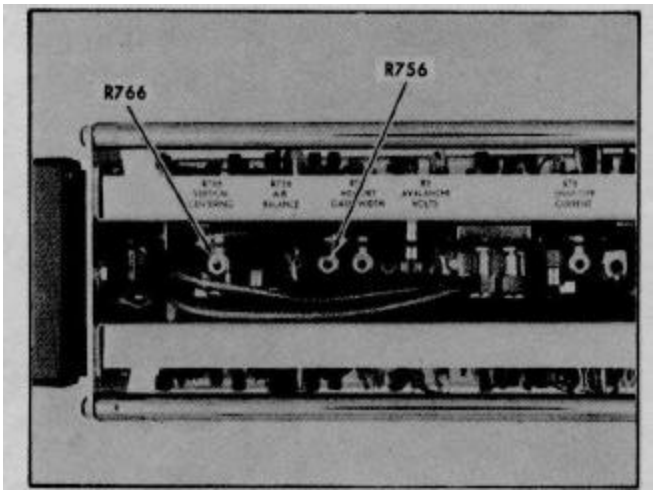

Fig. 8-24. A-B Bal control location, Step 18. Vertical Centering control location, Step 20.

e. Set the Type 3S1 Display Mode switch to CHAN B, the INTERNAL TRIGGER control to B, and move the signal cable to the B INPUT connector.

f. Set the 50 0 Amplitude Calibrator Volts control to 1.2 and repeat b and c on Channel B.

g. Check that the neon UNCAL lamps both operate when the associated mVolts/Div VARIABLE control is turned away from its CAL detent position. If a control white dot is not in agreement with the detent position, reposition the knob on the shaft.

20. Adjust Vertical Centering R766 and Check Vertical Position Indicating Lamps ◐

a. Remove any signal from the two input connectors. Free run the Timing Unit. Set both INVERT-NORMAL switches halfway between their normal positions and set the Display Mode switch to DUAL-TRACE.

b. Move both DC OFFSET controls. Neither trace should move. If one trace or the other moves, the associated INVERT-NORM switch is not properly between positions.

c. Set both POSITION controls halfway between the ends of rotation. If either white dot does not rest at top center, reposition the knob to locate the spot at the center position.

d. Check that the two traces appear near each other, but that they do not blend into one. Adjust the Vertical Centering control R766 (shown in Fig. 8-24) until the two traces straddle the graticule centerline.

e. Set both INVERT-NORM switches to NORM and the Display Mode switch to CHAN A. Move the trace above and below the graticule center horizontal line and check that the proper lamp is lighted by the time the trace has moved one division away from the centerline.

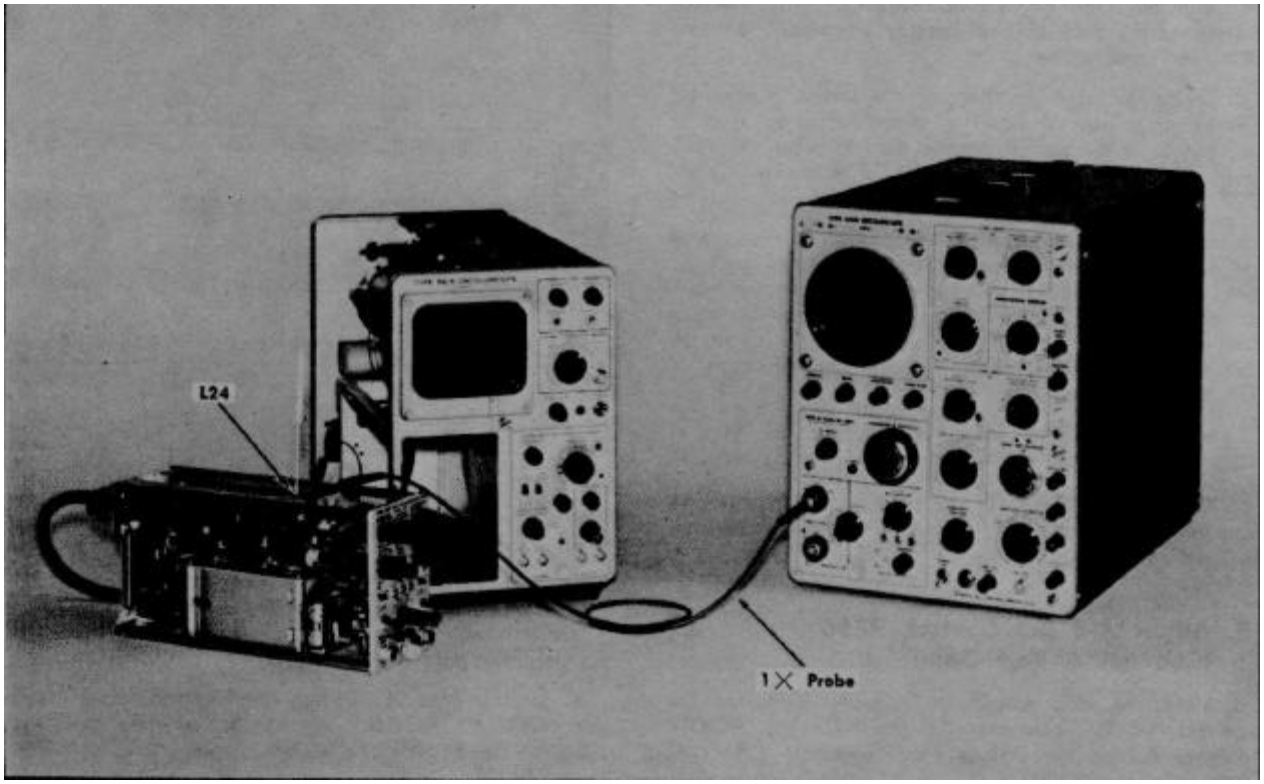

Fig. 8-25. Test Setup for Step 21.

Control Settings

Type 3S1	
Display Mode Switch	CHAN A
SMOOTH-NORMAL	NORMAL
INTERNAL TRIGGER	A
HORIZ PLUG-IN	**NON-SAMPLING 2B, 3B-SERIES**
Channel A	
A POSITION	Midrange
DC OFFSET	Optional
mVOLTS/DIV	200
VARIABLE	CAL
INVERT-NORM	NORM
Channel B	
B POSITION	Midrange
DC OFFSET	Optional
mVOLTS/DIV	200
VARIABLE	CAL
INVERT-NORM	NORM
Type 3T77A	
Horizontal Position	Midrange
Time/Div	2 *m*Sec
Variable	Calib detent position
Time Expander	X1
Dots/Div	100
Time Position	Optional
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	**Fully Clockwise**
Triggering Source	+Int
Recovery Time	Fully Counterclockwise
Test Oscilloscope	
Sweep Rate	**10 *m*sec/div**
Triggering	+Internal
Vertical	**10 mVolts/div (including 1X Probe)**

Connections

Place a 1X Probe on the Type W A Input connector.

21. Check and Adjust 100 kHz Free Run Frequency

a. Make the connections and control settings as stated following Fig. 8-25. Insert the coil adjusting tool (item 22 of equipment required) into L24, and hold the 1X Probe tip near L24 as shown in Fig. 8-25.

b. Obtain a stable test oscilloscope triggered display similar to Fig. 8-26. The signal coupling is through capacitance to the probe tip only, therefore it is not loading the oscillator circuit.

c. If the display produces other than 10 cycles in 10 divisions, adjust L24 until the Free Run oscillator frequency does produce 10 cycles in 10 divisions.

NOTE

As long as the Type 3S1 HORIZ PLUG-IN switch is at NON-SAMPLING 2B, 3B-SERIES, there will be no sampling display when the Timing Unit is a sampling unit. There can be a display if the Timing Unit is a real-time time base.

d. Remove the adjusting tool and the probe tip from the vicinity of L24. Leave the 1X Probe connected to the Type W unit. Set the Type 3S1 HORIZ PLUG-IN switch to SAMPLING 3T-SERIES.

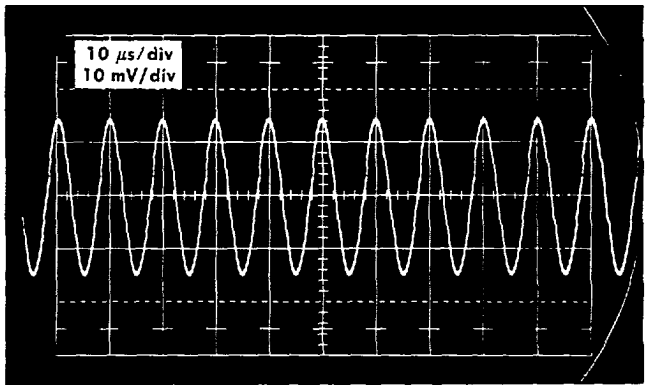

Fig. 8-26. Test oscilloscope display of Free Run oscillator frequency.

NOTES

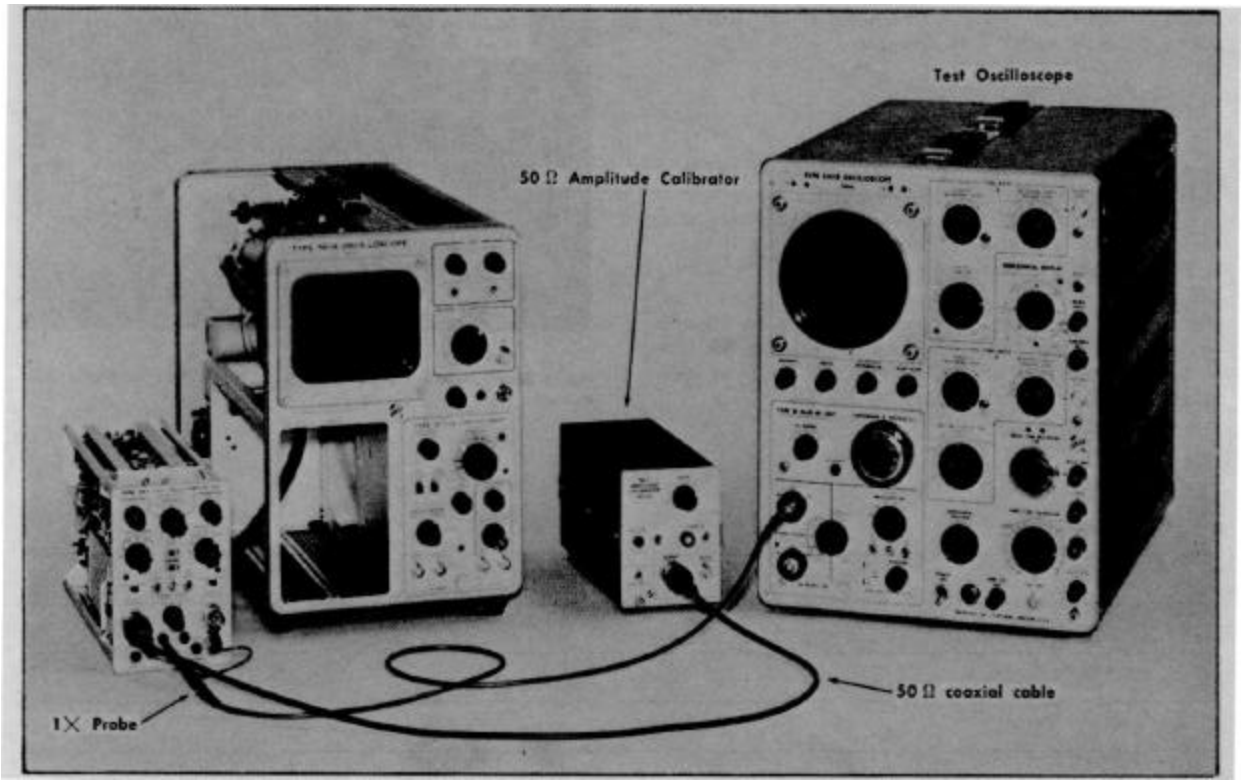

Fig. 8-27. Equipment and connections used in Step 22. Same equipment used in Step 23.

Control Settings

Type 3S1

Display Mode Switch	CHAN A
SMOOTH-NORMAL	NORMAL
INTERNAL TRIGGER	A
HORIZ PLUG-IN	**SAMPLING 3T-SERIES**

Channel A

A POSITION	Midrange
DC OFFSET	Zero volts out
mVOLTS/DIV	200
VARIABLE	CAL
INVERT-NORM	NORM

Channel B

B POSITION	Midrange
DC OFFSET	Zero volts out
mVOLTS/DIV	200
VARIABLE	CAL
INVERT-NORM	NORM

Type 3T77A

Horizontal Position	Midrange
Time/Div	2 *m*Sec
Variable	Calib detent position
Time Expander	X1
Dot/Div	100
Time Position	Optional
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	**Triggered display**
Triggering Source	**-Int**
Recovery Time	Fully Counterclockwise

50 W Amplitude Calibrator

Volts	.6

Test Oscilloscope

Sweep Rate	**Optional**
Triggering	**Free Run Trace**

Type W

Input Atten	**1**
Millivolts/Cm	**50**
Comparison Voltage	
Outer Dial	**6**
Variable Dial	0.00
Vc Range	0
Input Coupling	DC
Display	A-Vc

Connections

Place a 1X Probe on the Type W A Input connector. Connect the 50 Ω Amplitude Calibrator Output connector to the

Type 3S1 A INPUT connector with a 50-Ω coaxial cable. Connect the 1X Probe ground clip to the outer conductor of one of the Type 3S1 input connectors and touch the probe straight tip to the A OFFSET OUT jack.

22. Check Offset Circuit Operation

a. Make the connections and control settings called out following Fig. 8-27. Set the Type 3S1 Channel A DC OFFSET control so the test oscilloscope free run trace rests at zero volts.

b. Set the Type W Input Atten switch to infinity, and make certain the 1X Probe tip remains connected to the A OFFSET OUT jack. (If the probe tip loses its circuit connection, the test oscilloscope trace will probably go off screen.)

c. Obtain a stable triggered display on the Type 3S1 indicator oscilloscope CRT. Adjust the A POSITION control so the square wave top is exactly at the graticule centerline.

d. Set the Type W Vc Range switch to -11, and then turn the Type 3S1 Channel A DC OFFSET control clockwise until the square wave display bottom is exactly at the indicator oscilloscope graticule centerline. The test oscilloscope free run display should now be visible on the CRT. The deflection factor is 50 mV/div, or 0.833% per division; 1% is 1.2 major divisions. The trace must not be more than 2.4 divisions away from the graticule centerline, or not more than 2%.

e. Set the Type W Comparison Voltage outer dial to 10, and turn the Type 3S1 Channel A DC OFFSET control farther clockwise. The test oscilloscope trace must go upward post the graticule centerline before the DC OFFSET control reaches the end of its range, and the Type 3S1 square wave display bottom must go upward post the indicator oscilloscope plus 2-division graticule line (a total vertical travel of over 5 divisions).

f. Set the Type W Input Atten switch to 1, and remove the 1X Probe tip from the Type 3S1 A OFFSET OUT jack. Set the Type W Vc Range switch to 0.

g. With the Type 3S1 Channel A DC OFFSET control, return the square wave display so the top is at the graticule centerline: This set the DC OFFSET OUT voltage to essentially zero. Use the Type 3S1 A POSITION control and set the square wave display bottom at the plus 2-division graticule line.

h. Turn the Type 3S1 Channel A DC OFFSET control counterclockwise. The square wave display bottom must pass the minus 3-division graticule line before the control reaches the end of its range (a total downward travel of over 5 divisions).

i. Move the 50 Ω Amplitude Calibrator signal cable to the Type 3S1 B INPUT connector, and repeat the whole procedure on Channel B.

23. Check Internal Trigger Pickoff Signal Amplitude

a. Use the some equipment as connected at the end of step 22. The test oscilloscope deflection factor remains 50 mV/div. Change its sweep rate to 10 ms/div. Set the Type 3S1 INTERNAL TRIGGER switch to OFF. The 50 Ω Amplitude Calibrator connected to the B INPUT connector should be delivering a 0.6-volt square wave.

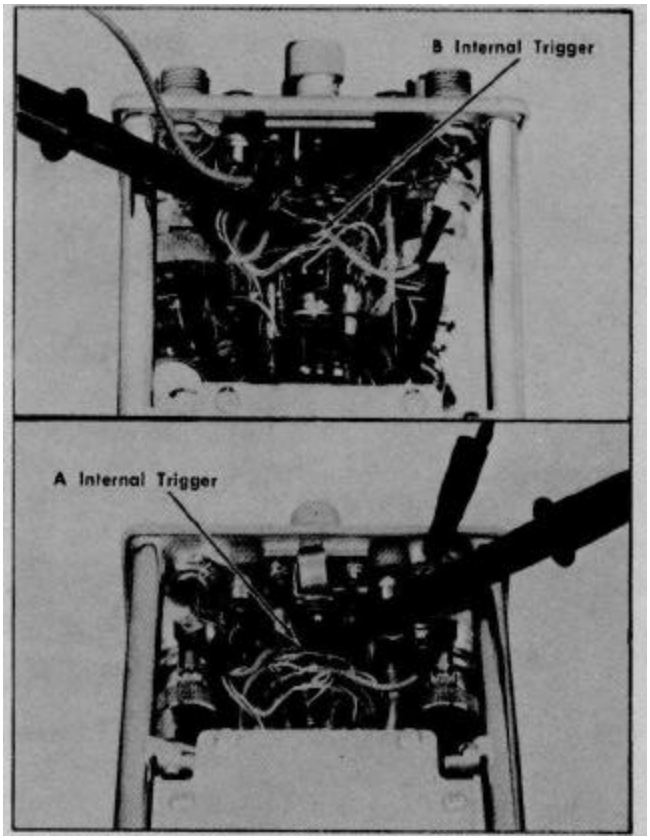

Fig. 8-28. Test oscilloscope probe positions for Step 23.

b. Turn the Type 3S1 upside down. Connect the test oscilloscope 1X Probe ground clip to the Type 3S1 chassis near the front panel, and touch the straight probe tip to the INTERNAL TRIGGER switch at the end of the coaxial cable that comes out of the B INPUT connector trigger pickoff. The proper probe tip position is shown in Fig. 8-28A.

c. Adjust the test oscilloscope triggering for a stable square wave display. The display peak to peak amplitude must be at least one division (12% = 0.96 divisions).

d. Move the 50 Ω Amplitude Calibrator signal cable to the Type 3S1 A INPUT connector. Move the 1X Probe tip to the end of the coaxial cable that comes out of the A INPUT connector trigger pickoff. The proper probe tip position is shown in Fig. 8-28B. The test oscilloscope square wave display must be at least one division peak to peak.

e. Remove the 1X probe and the coaxial signal cable from the Type 3S1.

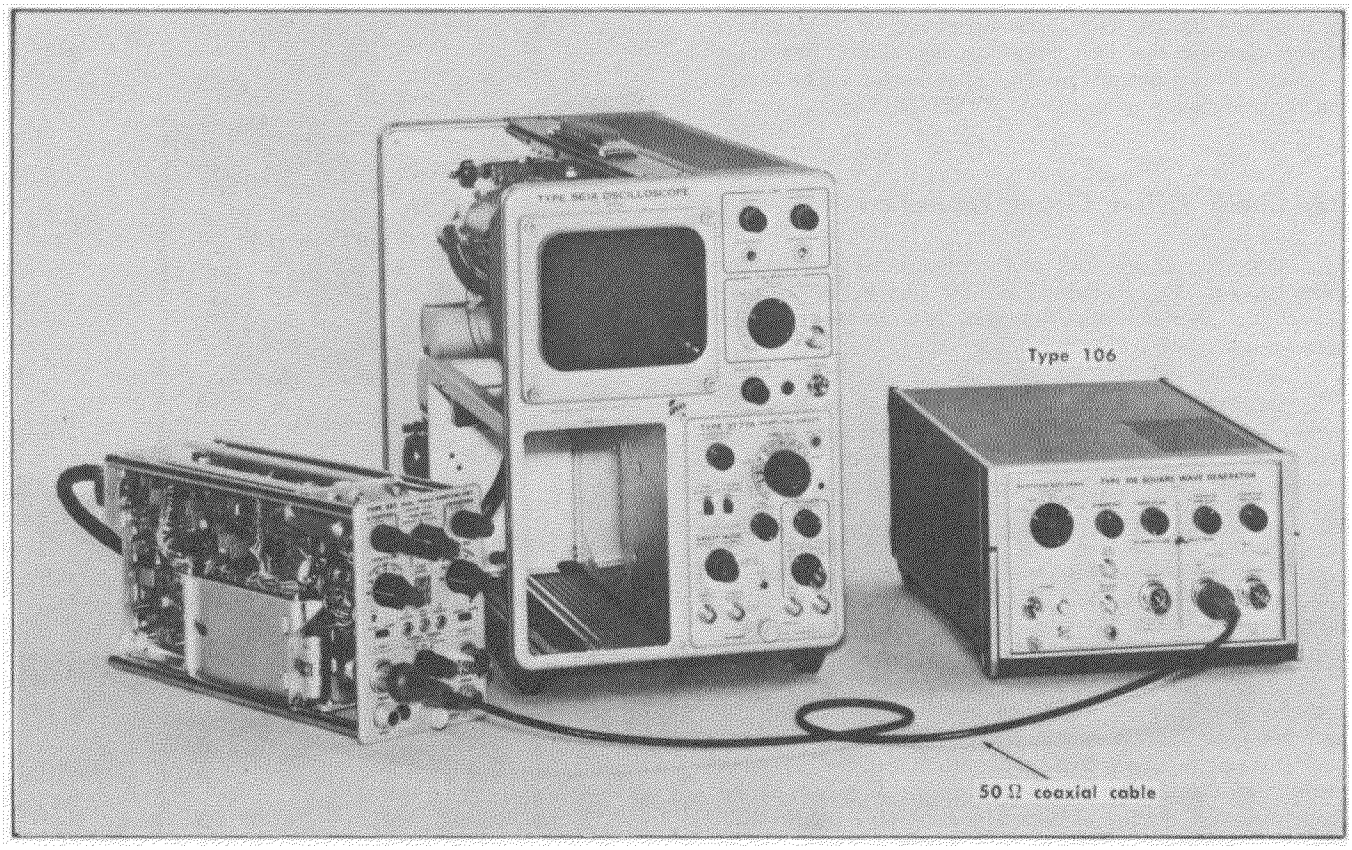

Fig. 8-29. Equipment and connections for Step 24.

Control Settings

Type 3S1

Display Mode Switch	**CHAN A**
SMOOTH-NORMAL	NORMAL
INTERNAL TRIGGER	A
HORIZ PLUG-IN	SAMPLING 3T-SERIES
Channel A	
A POSITION	Midrange
DC OFFSET	Midrange, centered trace
mVOLTS/DIV	200
VARIABLE	CAL
INVERT-NORM	NORM
Channel B	
B POSITION	Midrange
DC OFFSET	Midrange, centered trace
mVOLTS/DIV	200
VARIABLE	CAL
INVERT-NORM	NORM

Type 3T77A

Horizontal Position	Midrange
Time/Div	2 mSec
Variable	Calib detent position
Time Expander	X1
Dots/Div	100
Time Position	Optional
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	Triggered Display
Triggering Source	**+ Int**
Recovery Time	Fully counterclockwise

Type 106

Repetition Rate Range	100 kHz
Multiplier	1
Output selector	Fast Rise
+Transition Amplitude	Midrange

Connections

Install a 50 Ω coaxial cable between the Type 106 +Output connector and the Type 3S1 A INPUT connector. Use a GR to BNC male adapter at the Timing Unit external trigger input connector.

24. Check Trace Baseline Shift, 100 kHz to 30 Hz

a. Make the connections and control settings called out under Fig. 8-29. Adjust the Timing Unit for a stable triggered

display. Set the Type 106 + Transition Amplitude control for a one-division peak to peak display (200 mV).

b. Move the 50 Ω coaxial cable output end to the Timing Unit External Input connector and change the trigger selector switch to + External. The indicator display should now be a no-signal trace.

c. Set the Type 3S1 Channel A mVOLTS/DIV switch to 5 (it may be necessary to adjust the DC OFFSET control as the mVOLTS/DIV control is advanced, in order to keep the trace on the CRT). Position the trace to the graticule centerline.

d. Change the Type 106 signal rate to 30 Hz by setting the Repetition Rate Range switch to 10 Hz, and the Multiplier control to 3. The Type 3S1 indicator oscilloscope display must not move from the graticule centerline more than 10 mV, or no more than ±2 major divisions.

e. Repeat the above procedure for Channel B.

NOTE

Should either channel shift more than 10 mV vertically, and if such a shift is undesirable for the use the instrument will receive, change the four sampling gate diodes. Repeat this whole procedure beginning with step 4.

f. Leave the Type 106 connected to the Timing Unit for step 25.

25. Check Memory Slash (Dot Drift) at 20 Hz

a. With the equipment as connected at the end of step 24, set both Type 3S1 mVOLTS/DIV switches to 200. Set the Type 106 output to 20 Hz by setting the Multiplier control to 2. Set the Timing Unit Dots Per Div switch to 10 and check the indicator oscilloscope CRT focus for a display of sharp dots.

b. Check that the indicator oscilloscope dots do not move vertically more than 0.1 major division (a minor graticule division is 0.2 major division).

If the dots do drift more than 0.1 major division (appears as a long dot vertically), either the Memory diodes require replacement, or more likely, the Smoothing Balance adjustment is incorrect. Also, the Memory Field Effect Transistor or diodes D276-D277 can cause the dot slash. Perform the maintenance, and then repeat step 13 of this procedure.

c. Set the Display Mode switch to CHAN A and check the dot slash for Channel A. The dots must not be longer than 0.1 major division.

NOTES

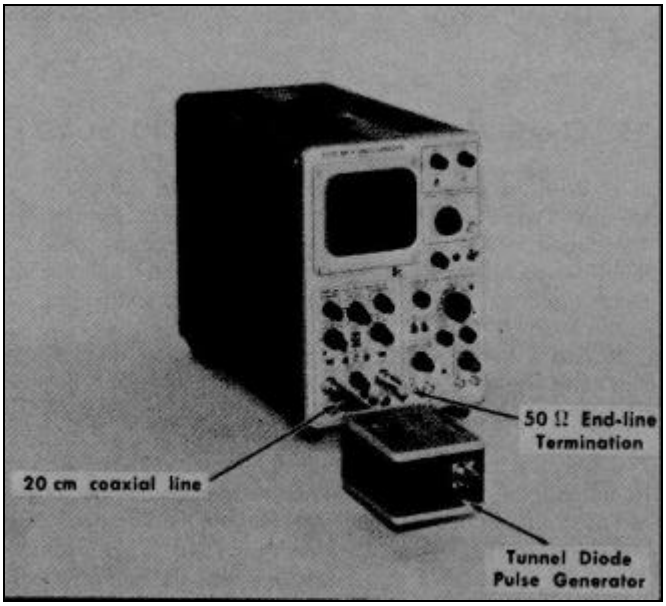

Fig. 8-30. Equipment and connections for Step 26.

Control Settings

Type 3S1	
Display Mode Switch	**DUAL TRACE**
SMOOTH-NORMAL	NORMAL
INTERNAL TRIGGER	A
HORIZ PLUG-IN	SAMPLING 3T-SERIES
Channel A	
A POSITION	Midrange
DC OFFSET	Centered display
mVOLTS/DIV	**100**
VARIABLE	CAL
INVERT-NORM	NORM
Channel B	
B POSITION	**Trace as in Fig. 8-31**
DC OFFSET	**Zero volts at B OFFSET OUT jack**
mVOLTS/DIV	**2**
VARIABLE	CAL
INVERT-NORM	NORM
Type 3T77A	
Horizontal Position	Midrange
Time/Div	**.5 nsec**
Variable	Calib detent Position
Time Expander	X 1

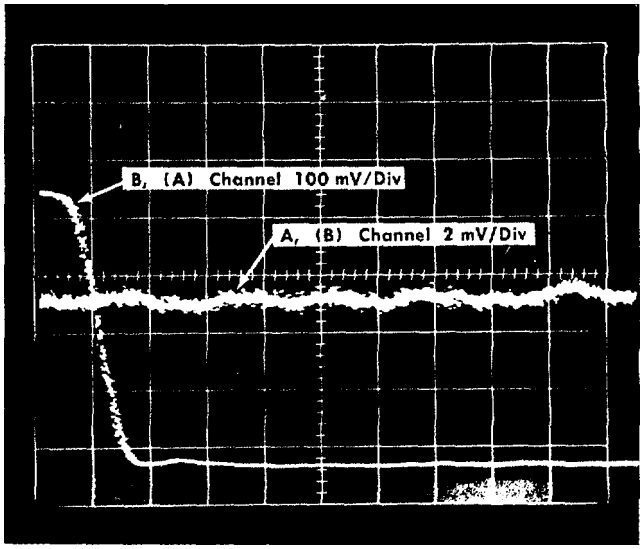

Fig. 8-31. Interchannel crosstalk waveforms. Step 26.

Dots/Div	100
Time Position	Display as in Fig. 8-31
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	Triggered display
Triggering Source	-Int
Recovery Time	Fully counterclockwise
Tunnel Diode Pulse Generator	
On, with bias set for clean display	

Connections

Connect the Tunnel Diode Pulse Generator Pulse Output connector to the Type 3S1 A INPUT connector with a GR 874-L20, 20 cm 50 0 coaxial air line. Install a 50 Ω termination on the Type 35S1 B INPUT connector.

26. Check Interchannel Crosstalk

a. Make the connections and control settings listed under Fig. 8-30. It may be necessary to adjust the Channel A DC OFFSET control to position the display correctly. Adjust the Timing Unit Trigger Sensitivity control for a stable display. The Tunnel Diode Pulse Generator negative pulse and Channel B trace should both be visible, similar to Fig. 8-31.

The maximum peak to peak signal permitted to show in the Channel B trace is 1% of the Tunnel Diode Pulser signal amplitude at the step transition. The crosstalk can show anywhere following the negative step.

There is no need to reverse channels, as the crosstalk circuit is identical, and the display should be very similar.

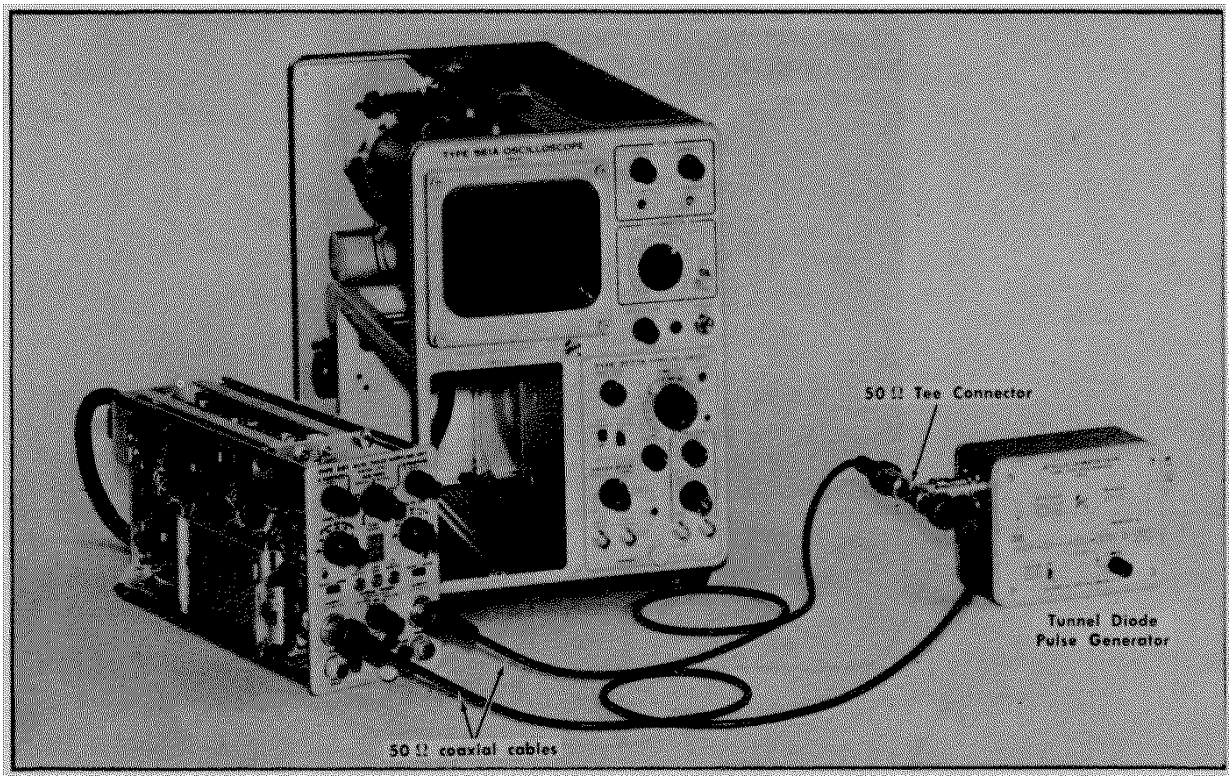

Fig. 8-32. Equipment and connections for Step 27.

Control Settings

Type 3S1

Display Mode Switch	DUAL TRACE
SMOOTH-NORMAL	**SMOOTH**
INTERNAL TRIGGER	A
HORIZ PLUG-IN	SAMPLING 3T-SERIES

Channel A

A POSITION	Midrange
DC OFFSET	Display as in Fig. 8-33A
mVOLTS/DIV	100
VARIABLE	CAL
INVERT-NORM	NORM

Channel B

B POSITION	Midrange
DC OFFSET	Display like Fig. 8-33A
mVolts/DIV	**100**
VARIABLE	CAL
INVERT-NORM	NORM

Type 3T77A

Horizontal Position	Midrange
Time/Div	**1 nsec**
Variable	Calib detent Position
Time Expander	**X10**
Dots/Div	100
Time Position	Display as in Fig. 8-33A
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	Triggered display
Triggering Source	-Int
Recovery Time	Fully counterclockwise

Tunnel Diode Pulse Generator

On, with bias set for clean display

Connections

Connect two 5 ns signal delay 50 Ω coaxial cables to a GR 874-T. Install the Tee onto the Tunnel Diode Pulse Generator Pulse Output connector. Install the cables other ends to the two Type 3S1 input connectors.

27. Check Co-Channel Time Coincidence

NOTE

This step should be performed any time there has been maintenance applied to the input circuits, or to the circuit between the gate generator and a sampling bridge. If a delay line is changed or if T139 (T439) is changed, perform this setup. Minor changes in the time coincidence error can be made by changing the length of the leads to T139 (T439). For example, if Channel A is over 30 ps later than Channel B, shortening the leads of T139 will reduce the time coincidence error.

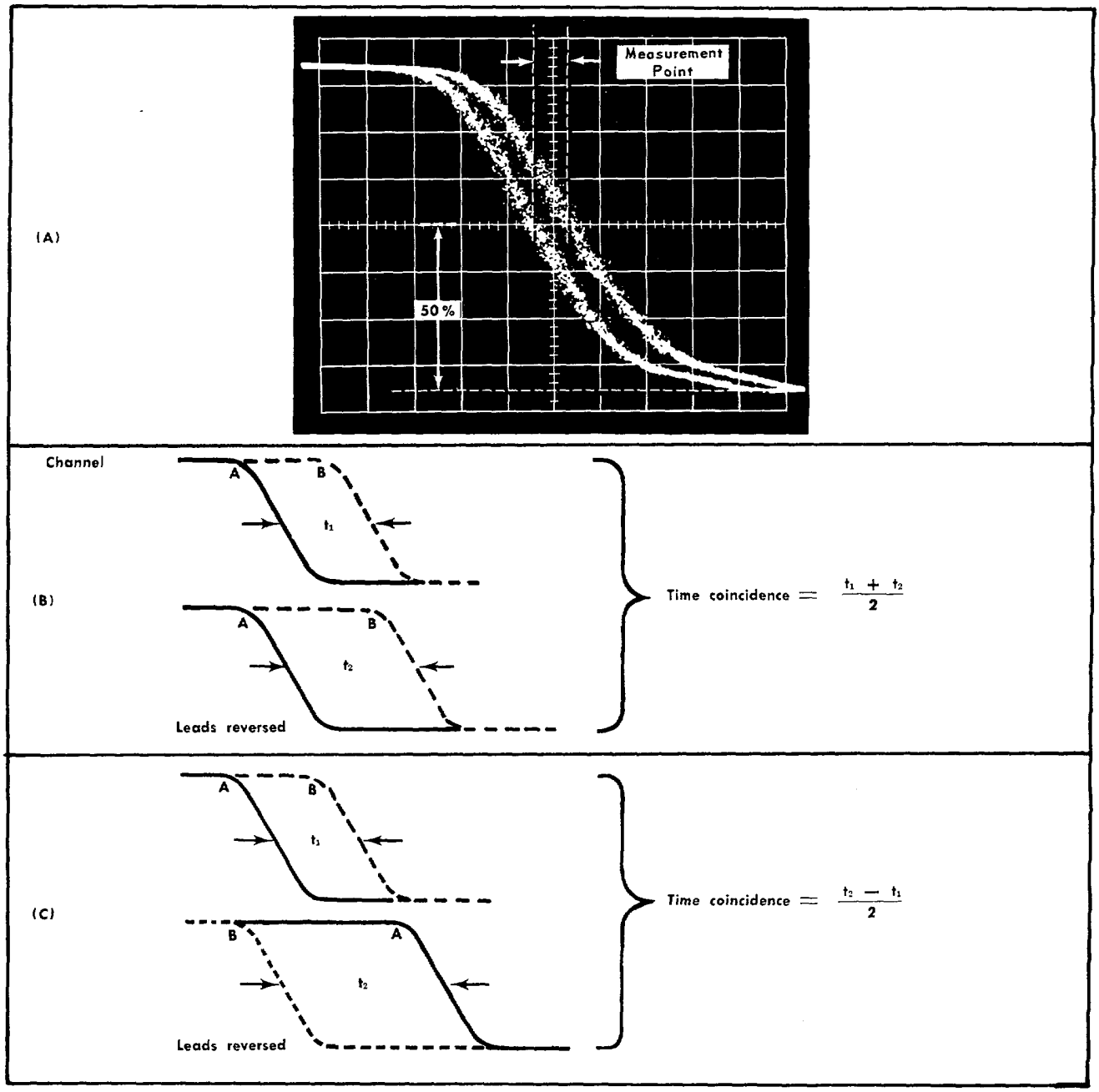

Fig. 8-33. Calculating the Co-Channel time coincidence error, Step 27.

a. Make the connections and control settings listed following Fig. 8-32. Adjust the Timing Unit Trigger Sensitivity control for a stable display. Adjust the Time position control for a centered display.

b. Carefully position the two displays so they occupy the same vertical position in their horizontal parts. This leaves only their horizontal difference obvious.

c. Measure and record the time difference between the two displays at the 50% amplitude points [the sweep rate is 100 ps/div).

d. Move the Channel B display vertically and note whether it is on the right or left of the Channel A display.

e. Reverse the signal cables to the Type 3S1 two input connectors and again measure and record the time difference between the two displays at their 50% points.

f. Move the Channel B display vertically and note whether it is on the right or left of the Channel A display.

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Calculating the Time Coincidence Error

If the two display did **not** interchange position when the input cables were reversed, add the two recorded times and divide by 2 to obtain the time coincidence number. See Fig. 8-33.

If the two displays **did** interchange position when the input cables were reversed, subtract the two recorded times and divide by 2 to obtain the time coincidence number. See Fig. 8-33C.

The time coincidence error must not be greater than 30 ps.

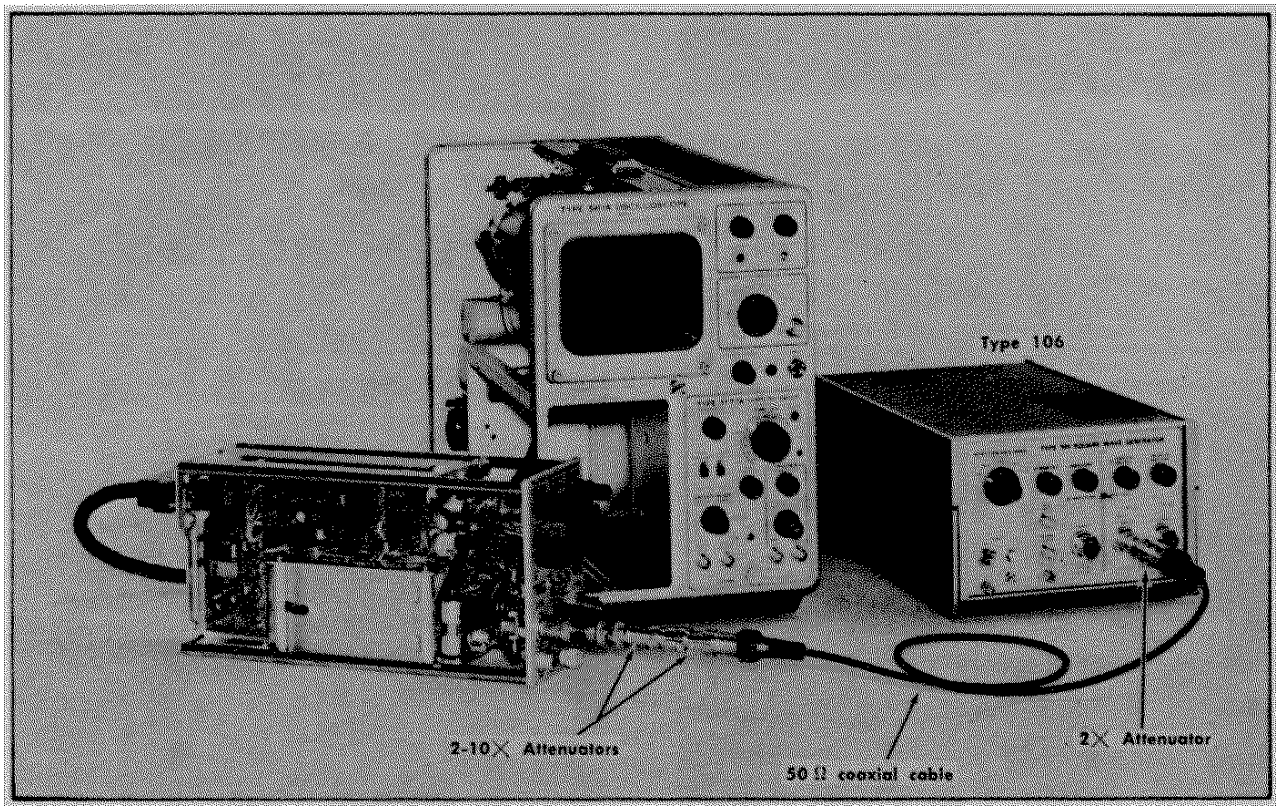

Fig. 8-34. Equipment and connections for Step 28.

Control Settings

Type 3S1	
Display Mode Switch	**CHAN A**
SMOOTH-NORMAL	**NORMAL**
INTERNAL TRIGGER	**OFF**
HORIZ PLUG-IN	SAMPLING 3T-SERIES
Channel A	
A POSITION	Midrange
DC OFFSET	Zero volts at A OFFSET OUT
mVOLTS/DIV	**2**
VARIABLE	CAL
INVERT-NORM	NORM
Channel B	
B POSITION	Midrange
DC OFFSET	Zero volts at B OFFSET OUT
mVOLTS/DIV	**2**
VARIABLE	CAL
INVERT-NORM	NORM
Type 3T77A	
Horizontal Position	Midrange
Time/Div	**1 nSec**
Variable	Calib detent position
Time Expander	X 1
Dots/Div	100
Time Position	Optional
Sweep Mode	Normal
Manual Scan or Ext Atten	Optional
Trigger Sensitivity	**Fully Clockwise**
Triggering Source	**Optional**
Recovery Time	**Fully clockwise**
Type 106	
Repetition Rate Range	100 Hz
Multiplier	1 (100 Hz signal)
Output Selector Switch	Fast Rise
+ Transition Amplitude	Midrange

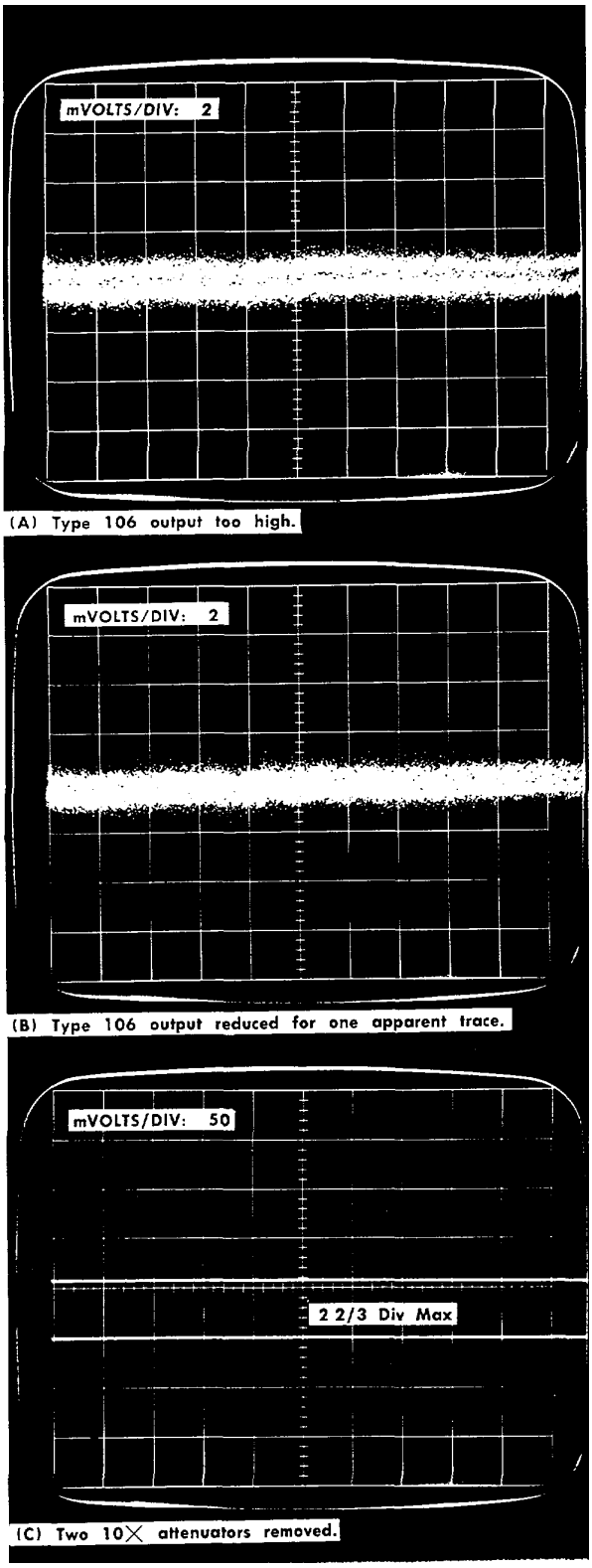

Fig. 8-35. Tangential noise measurement display. SMOOTH-NORMAL switch at NORMAL Step 28.

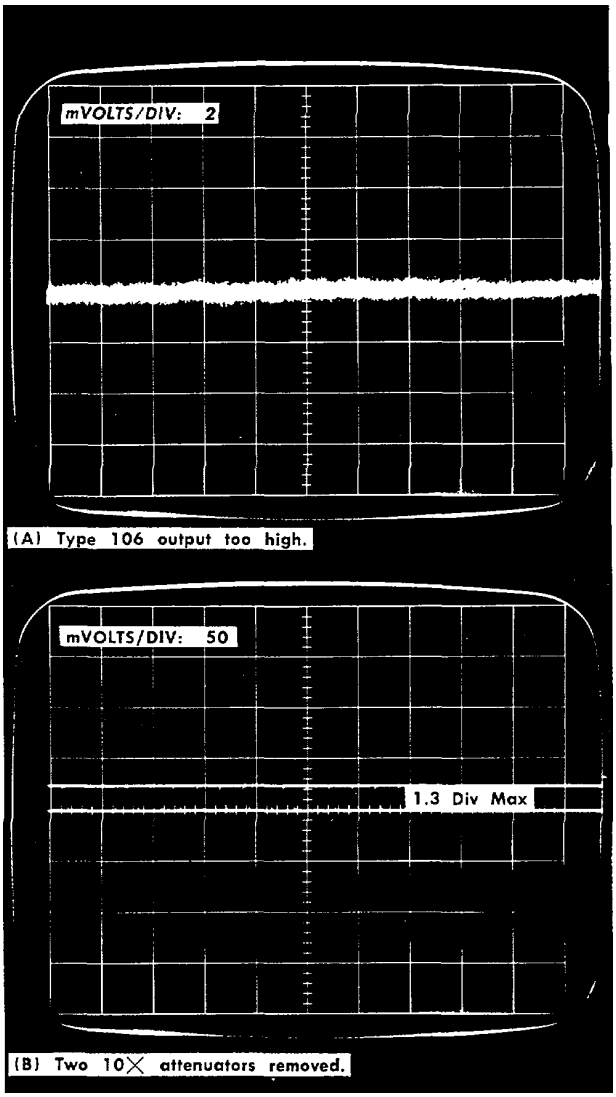

Fig. 8-36. Tangential noise measurement, SMOOTH-NORMAL switch at SMOOTH. Step 28.

Connections

Install a 2X attenuator at the Type 106 + Output connector. Install a 50 Ω coaxial cable to the 2X attenuator. Install two 10X attenuators on the cable end, and connect the attenuators to the Type 3S1 A INPUT connector.

28. Check Tangential Noise

NOTE

When making a visual noise reading from a sampling display, the eye interprets a noise value which is neither the RMS nor the peak to peak value. Since most observers agree that the displayed noise value is approximately 3 times the RMS value, the Tangential Noise here defined

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is 3 times the RMS value. (The measurement technique given produces acceptable agreement between various operators as to the instrument's noise value.)

a. Make the connections and set the controls as listed under Fig. 8-34. Obtain a display similar to Fig: 8-35A where two traces are obvious. This is really a display of the square wave generator signal amplitude, highly attenuated.

b. Reduce the Type 106 output amplitude until the two traces blend together as one wide trace as shown in Fig. 8-35B.

c. Remove the two 10X attenuators from the signal cable and set the Channel A mVOLTS/DIV control to 50. Install the signal cable back onto the A INPUT connector. The display will be two lines, similar to Fig. 8-35C. The display deflection factor for noise is now 0.75 mV. Thus, the 2 mV tangential noise limit requires that the two traces be no more than 22/ divisions apart

Determining Tangential Noise Deflection Factor

The noise displays have a noise deflection factor based upon the signal amplitude, the Type 3S1 mVOLTS/DIV switch setting, the fact that the final trace separation is twice the RMS noise, and that the tangential noise is then 3 times the RMS noise. The setting of the square wove generator signal amplitude so that the two traces appear as one sets the trace separation to twice the RMS noise. The procedure used here then permits a noise deflection factor to be determined by dividing the input 50 mV/div deflection factor by 100 (the change in signal amplitude caused by removing two 10X attenuators), dividing again by 2 (trace separation is twice the RMS noise) and then multiplying by 3 (tangential noise is 3 times the RMS noise. This gives a tangential noise deflection factor of 0.75 mV/Div.

d. Reinstall the two 10X attenuators in the signal cable path. Set the Channel A mVOLTS/DIV switch to 2. Set the SMOOTH-NORMAL switch to SMOOTH and reduce the square wove generator output until the two traces blend as one, similar to Fig. 8-36A. (The Type 106 output amplitude should now be less than in (b) above.)

e. Remove the two 10X attenuators from the signal path and set the Channel A mVOLTS/DIV switch to 50. Reconnect the signal cable. The two traces must not be more than 1.3 divisions apart.

NOTE

If noise is excessive, the Avalanche Volts control requires adjustment. Do not change the Avalanche Volts control until after checking Channel B noise. Then, the noisier channel dictates the needed noise reduction.

f. Move the signal cable to the Type 3S1 8 lNPUT connector; set the Display Mode switch to CHAN B, and repeat the whole step on Channel B.

NOTE

If it is decided to readjust the Avalanche Volts control, again perform steps 5, 6, 10 and 11.

Turn off the indicator oscilloscope power, remove the flexible extension cable and insert the Type 3S1 into the oscilloscope. The Type 3S1 is ready for use.

NOTES

PARTS LIST ABBREVIATIONS

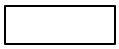
BHB	binding head brass	lg	length or long
BHS	binding head steel	met	metal
cap.	capacitor	mtg hdw	mounting hardware
cer	ceramic	OD	outside diameter
comp	composition	OHB	oval head brass
conn	connector	OHS	oval head steel
CRT	cathode-ray tube	P/O	part of
csk	countersunk	PHB	pan head brass
DE	double end	PHS	pan head steel
dia	diameter	plstc	plastic
div	division	PMC	paper, metal cased
elect	electrolytic	poly	polystyrene
EMC	electrolytic, metal cased	prec	precision
EMT	electrolytic, metal tubular	PT	paper, tubular
ext	external	PTM	paper or plastic, tubular, molded
F & I	focus and intensity	RHB	round head brass
FHB	flat head brass	RHS	round head steel
FHS	flat head steel	SE	single end
Fil HB	fillister head brass	SN or S/N	serial number
Fi HS	fillis ter head steel	S or SW	switch
h	height or high	TC	temperature compensated
hex.	hexagonal	THB	truss head brass
HHB	hex head brass	thk	thick
HHS	hex head steel	THS	truss head steel
HSB	hex socket brass	tub.	tubular
HSS	hex socket steel	var	variable
ID	inside diameter	w	wide or width
inc	incandescent	WW	wire-wound
int	internal		

PARTS PROVISIONING LIST

REPLACEMENT PARTS

To obtain replacement parts, find the manufacturer's part number and description in this manual and then refer to the appropriate Repair Parts and Special Tools List (RPSTL) TM. In the RPSTL, find the assembly or subassembly first and then the description which corresponds with that in this manual. Under the description in the RPSTL find the manufacturer's part number, and then order the part by the listed Federal Stock Number. If the part is not listed in the RPSTL, it should be requisitioned from the NICP in accordance with AR 725-50.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number
*000-0000-00	Asterisk preceding Tektronix Part Number indicates manufactured by or for Tektronix, Inc., or reworked or checked components.
Use 000-0000-00	Part number indicated is direct replacement.
	Screwdriver adjustment.
	Control, adjustment or connector.

SECTION 9
ELECTRICAL PARTS LIST

Values are fixed unless marked Variable.

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Description			
				Bulbs			
B296	150-0035-00			Neon, A1D T2			
B596	150-0035-00			Neon, A1D T2			
B798	150-0035-00			Neon, A1D T2			
B799	150-0035-00			Neon, A1D T2			
				Capacitors			
Tolerance ±20% unless otherwise indicated.							
C3	283-0079-00			0.01 μF	Cer	250 V	
C10	281-0613-00			10 pF	Cer	200 V	10%
C14	283-0094-00			27 pF	Cer	200 V	10%
C20	290-0134-00			22 μF	Elect.	15 V	
C25	283-0059-00			1 μF	Cer	25 V	+80% -20%
C26	283-0593-01			0.01 μF	Mica	100 V	1%
C27	283-0593-01			0.01 μF	Mica	100 V	1%
C35	283-0108-00			220 pF	Cer	200 V	10%
C36	283-0084-00			270 pF	Cer	1000 V	5%
C41	283-0076-00			27 pF	Cer	500 V	10%
C44	283-0003-00			0.01 μF	Cer	150 V	
C50	281-0509-00			15 pF	Cer	500 V	10%
C56	283-0054-00			150 pF	Cer	200 V	5%
C70	283-0135-00			100 pF	Cer		
C72	283-0067-00			0.001 μF	Cer	200 V	10%
C77	290-0134-00			22 μF	Elect.	15 V	
C78	283-0135-00			100 pF	Cer		
C79	283-0135-00			100 pF	Cer		
C109	283-0110-00			0.005 μF	Cer	150 V	
C112	283-0110-00			0.005 μF	Cer	150 V	
C113	283-0079-00			0.01 μF	Cer	250 V	
C115	283-0032-00			470 pF	Cer	500 V	5%
C116	283-0065-00			0.001 μF	Cer	100 V	5%
C120	283-0059-00			1 μF	Cer	25 V	+80% -20%
C128	283-0059-00			1 μF	Cer	25 V	+80% -20%
C130	281-0064-00			0.25-1.5 pF, Var	Tub.		
C131	281-0064-00			0.25-1.5 pF, Var	Tub.		
C132	283-0032-00			470 pF	Cer	500 V	5%
C133	281-0043-00			0.7-3 pF, Var	Tub.		
C135	283-0069-00	B010100	B079999	15 pF	Cer	50 V	
C135	283-0166-00	B080000		15 pF	Cer	50 V	5%
C137	283-0067-00			0.001 μF	Cer	200 V	10%

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Capacitors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
C138	283-0069-00	B010100	B079999	15 pF	Cer	50 V	
C138	283-0166-00	B080000		15 pF	Cer	50 V	5%
C142	281-0516-00			39 pF	Cer	500 V	10%
C147	283-0067-00			0.001 mF	Cer	200 V	10%
C151	283-0067-00			0.001 mF	Cer	200 V	10%
C152	283-0065-00			0.001 mF	Cer	100 V	5%
C156	283-0059-00			1 mF	Cer	25 V	+80% -20%
C160	283-0059-00			1 mF	Cer	25 V	+80% -20%
C161	283-0026-00			0.2 mF	Cer	25 V	
C162	283-0051-00			0.0033 mF	Cer	100 V	5%
C172	283-0115-00			47 pF	Cer	200 V	5%
C176	283-0026-00			0.2 mF	Cer	25 V	
C181	283-0067-00			0.001 mF	Cer	200 V	10%
C190	281-0613-00			10 pF	Cer	200 V	10%
C194	281-0613-00			10 pF	Cer	200 V	10%
C209	281-0512-00			27 pF	Cer	500 V	
C202	283-0059-00			1 mF	Cer	25 V	+80% -20%
C207	283-0004-00			0.02 mF	Cer	150 V	
C221	283-0026-00			0.2 mF	Cer	25 V	
C230	283-0594-00			0.001 mF	Mica	100 V	1%
C232	283-0594-00			1 mF	Cer	25 V	+80% -20%
C243	283-0594-00			0.001 mF	Cer	100 V	
C247	283-0023-00			0.1 mF	Cer	10 V	10%
C253	283-0094-00			27 pF	Cer	200 V	10%
C261	283-0059-00			1 mF	Cer	25 V	+80% -20%
C267	283-0059-00			1 mF	Cer	25 V	+80% -20%
C272	283-0026-00			0.2 mF	Cer	25 V	
C274	283-0026-00			0.2 mF	Cer	25 V	
C276	285-0000-00			160 pF	Glass	500 V	1%
C295	283-0003-00			0.01 mF	Cer	150 V	
C307	283-0144-00			33 pF	Cer	500 V	1%
C415	283-0032-00			470 pF	Cer	500 V	5%
C416	283-0065-00			0.001 mF	Cer	100 V	5%
C420	283-0059-00			1 mF	Cer	25 V	+80% -20%
C428	283-0059-00			1 mF	Cer	25 V	+80% -20%
C430	281-0064-00			0.25-1.5 pF, Var	Tub.		
C431	281-0064-00			0.25-1.5 pF, Var	Tub.		
C432	283-0032-00			470 pF	Cer	500 V	5%
C433	281-0043-00			0.7-3 pF, Var	Tub.		
C435	283-0069-00	B010100	B079999	15 pF	Cer	50 V	
C435	283-0166-00	B080000		15 pF	Cer	50 V	5%
C437	283-0067-00			0.001 mF	Cer	200 V	10%
C438	283-0069-00	B010100	B079999	15 pF	Cer	50 V	
C438	283-0166-00	B080000		15 pF	Cer	50 V	5%
C442	281-0516-00			39 pF	Cer	500 V	10%
C447	283-0067-00			0.001 mF	Cer	200 V	10%
C451	283-0067-00			0.001 m F	Cer	200 V	10%
C452	283-0065-00			0.001 mF	Cer	100 V	5%
C456	283-0059-00			1 mF	Cer	25 V	+80% -20%
C460	283-0059-00			1 mF	Cer	25 V	+80% -20%
C461	283-0026-00			0.2 mF	Cer	25 V	
C462	283-0051-00			0.0033 mF	Cer	100 V	5%

Capacitors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
C472	283-0115-00			47 pF	Cer	200 V 5%
C476	283-0026-00			0.2 mF	Cer	25 V
C481	283-0067-00			0.001 mF	Cer	200 V 10%
C490	281-0613-00			10 pF	Cer	200 V 10%
C494	281-0613-00			10 pF	Cer	200 V 10%
C509	281-0512-00			27 pF	Cer	500 V
C502	283-0059-00			1 mF	Cer	25 V +80% -20%
C507	283-0004-00			0.02 mF	Cer	150 V
C521	283-0026-00			0.2 mF	Cer	25 V
C530	283-0594-00			0.001 mF	Mica	100 V 1%
C532	283-0059-00			1 mF	Cer	25 V +80% -20%
C543	283-0594-00			0.001 mF	Cer	100 V
C547	283-0023-00			0.1 mF	Cer	10 V 10%
C543	283-0594-00	XB100000		0.001 mF	Mica	100 V 1%
C547	283-0023-00	XB100000		0.1 mF	Cer	10 V
C553	283-0094-00	B100000		27 pF	Cer	200 V 10%
C561	283-0059-00			1 mF	Cer	25 V +80% -20%
C567	283-0059-00			1 mF	Cer	25 V +80% -20%
C572	283-0026-00			0.2 mF	Cer	25 V
C574	283-0026-00			0.2 mF	Cer	25 V
C576	285-0000-00			160 pF	Glass	500 V 1%
C595	283-0003-00			0.01 mF	Cer	150 V
C607	283-0144-00			33 pF	Cer	500 V 1%
C702	283-0128-00			100 pF	Cer	500 V 5%
C713	283-0059-00			1 mF	Cer	25 V +80% -20%
C719	283-0144-00			33 pF	Cer	500 V 1%
C723	283-0059-00			1 mF	Cer	25 V +80% -20%
C729	283-0144-00			33 pF	Cer	500 V 1%
C779	281-0501-00			4.7 pF	Cer	500 V ±1 pF
C782	283-0026-00			0.2 mF	Cer	25 V
C816	283-0092-00			0.03 mF	Cer	200 V +80% -20%
C822	290-0333-00			300 mF	Elect.	25 V +75% -10%
C828	283-0076-00			27 pF	Cer	500 V 10%
C839	290-0167-00			10 mF	Elect.	15 V
C853	283-0059-00			1 mF	Cer	25 V +80% -20%
C855	283-0059-00	B010100	B039999X	1 mF	Cer	25 V +80% -20%
C861	283-0059-00			1 mF	Cer	25 V +80% -20%
C863	283-0059-00			1 mF	Cer	25 V +80% -20%
C865	283-0059-00			1 mF	Cer	25 V +80% -20%
C867	283-0059-00			1 mF	Cer	25 V +80% -20%
C881	283-0067-00			0.001 mF	Cer	200 V 10%
C882	283-0067-00			0.001 mF	Cer	200 V 10%

Diodes

D1	152-0141-02		Silicon	1N4152
D31	* 152-0185-00		Silicon	Replaceable by 1N4152
D37	* 152-0185-00		Silicon	Replaceable by 1N4152
D41	* 152-0233-00		Silicon	Tek Spec
D57	* 152-0185-00		Silicon	Replaceable by 1N4152
D59	* 152-0185-00		Silicon	Replaceable by 1N4152

Diodes *(cont)*

Ckt. No.		Tektronix Part No.	Serial/Model No. Eff	Disc	Description
D73	*	152-0252-00			Snap-Off Pre-tested
D137A,B,C,D	*	152-0314-00			Silicon Tek Spec
D139		152-0141-02			Silicon 1N4152
D156	*	152-0185-00			Silicon Replaceable by 1N4152
D175	*	152-0185-00			Silicon Replaceable by 1N4152
D200	*	152-0185-00			Silicon Replaceable by 1N4152
D202	*	152-0185-00			Silicon Replaceable by 1N4152
D210	*	152-0185-00			Silicon Replaceable by 1N4152
D214	*	152-0185-00			Silicon Replaceable by 1N4152
D216	*	152-0185-00			Silicon Replaceable by 1N4152
D231		152-0195-00			Zener 1N751A 0.4 W, 5.1 V, 5%
D232	*	152-0185-00			Silicon Replaceable by 1N4152
D233	*	152-0185-00			Silicon Replaceable by 1N4152
D234	*	152-0185-00			Silicon Replaceable by 1N4152
D236	*	152-0185-00			Silicon Replaceable by 1N4152
D237	*	152-0323-00			Silicon Tek Spec
D238	*	152-0185-00			Silicon Replaceable by 1N4152
D239	*	152-0323-00			Silicon Tek Spec
D243	*	152-0185-00			Silicon Replaceable by 1N4152
D254	*	152-0185-00			Silicon Replaceable by 1N4152
D256	*	152-0185-00			Silicon Replaceable by 1N4152
D276	*	152-0323-00			Silicon Tek Spec
D277	*	152-0323-00			Silicon Tek made
D286	*	152-0185-00			Silicon Replaceable by 1N4152
D306	*	152-0185-00			Silicon Replaceable by 1N4152
D310	*	152-0185-00			Silicon Replaceable by 1N4152
D316	*	152-0185-00			Silicon Replaceable by 1N4152
D317		152-0034-00	B010100	B069999	Zener 1N753 0.4 W, 6.2 V, 5%
D317		152-0280-00	B070000		Zener 1N753A 0.4W, 6.2 V, 5%
D331	*	152-0185-00			Silicon Replaceable by 1N4152
D437A,B,C,D	*	152-0314-00			Silicon Tek Spec
D439		152-0141-02			Silicon 1N4152
D456	*	152-0185-00			Silicon Replaceable by 1N4152
D475	*	152-0185-00			Silicon Replaceable by 1N4152
D500	*	152-0185-00			Silicon Replaceable by 1N4152
D502	*	152-0185-00			Silicon Replaceable by 1N4152
D510	*	152-0185-00			Silicon Replaceable by 1N4152
D514	*	152-0185-00			Silicon Replaceable by 1N4152
D516	*	152-0185-00			Silicon Replaceable by 1N4152
D531		152-0195-00			Zener 1N751A 0.4 W, 5.1 V, 5%
D532	*	152-0185-00			Silicon Replaceable by 1N4152
D533	*	152-0185-00			Silicon Replaceable by 1N4152
D534	*	152-0185-00			Silicon Replaceable by 1N4152
D536	*	152-0185-00			Silicon Replaceable by 1N4152
D537	*	152-0323-00			Silicon Tek Spec

Diodes *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
D538	* 152-0185-00			Silicon Replaceable by 1N4152
D539	* 152-0323-00			Silicon Tek Spec
D543	* 152-0185-00			Silicon Replaceable by 1N4152
D554	* 152-0185-00			Silicon Replaceable by 1N4152
D556	* 152-0185-00			Silicon Replaceable by 1N4152
D576	* 152-0323-00			Silicon Tek Spec
D577	* 152-0323-00			Silicon Tek Spec
D586	* 152-0185-00			Silicon Replaceable by 1N4152
D606	* 152-0185-00			Silicon Replaceable by 1N4152
D610	* 152-0185-00			Silicon Replaceable by 1N4152
D616	* 152-0185-00			Silicon Replaceable by 1N4152
D617	152-0034-00	B010100	B069999	Zener 1N753 0.4 W, 6.2 V, 10%
D617	152-0280-00	B070000		Zener 1N753A 0.4 W, 6.2 V, 5%
D701	* 152-0233-00			Silicon Tek Spec
D705	* 152-0185-00			Silicon Replaceable by 1N4152
D706	* 152-0185-00			Silicon Replaceable by 1N4152
0709	* 152-0185-00			Silicon Replaceable by 1N4152
D714	* 152-0185-00			Silicon Replaceable by 1N4152
D715	* 152-0185-00			Silicon Replaceable by 1N4152
D724	* 152-0185-00			Silicon Replaceable by 1N4152
D726	* 152-0185-00			Silicon Replaceable by 1N4152
D750	* 152-0185-00			Silicon Replaceable by 1N4152
D751	* 152-0185-00			Silicon Replaceable by 1N4152
D760	* 152-0185-00			Silicon Replaceable by 1N4152
D761	* 152-0185-00			Silicon Replaceable by 1N4152
D774	* 152-0185-00			Silicon Replaceable by 1N4152
D782	152-0166-00			Zener 1N753A 0.4 W, 6.2 V, 5%
D784	* 152-0185-00			Silicon Replaceable by 1N4152
D791	* 152-0185-00			Silicon Replaceable by 1N4152
D792	* 152-0185-00			Silicon Replaceable by 1N4152
D821A,B,C,D (4)	* 152-0107-00			Silicon Replaceable by 1N647
D827	152-0195-00			Zener 1N751 0.4 W, 5.1 V, 5%
D829	* 152-0185-00			Silicon Replaceable by 1N4152
D891	* 152-0107-00			Silicon Replaceable by 1N647
D892	* 152-0107-00			Silicon Replaceable by 1N647
D894	* 152-0107-00			Silicon Replaceable by 1N647
D895	* 152-0107-00			Silicon Replaceable by 1N647
D897	* 152-0107-00			Silicon Replaceable by 1N647
D898	* 152-0107-00			Silicon Replaceable by 1N647

Connectors

J1	131-0391-00	Coax, 50 Ω male
P11	131-0149-00	24 contact, male
P12	131-0149-00	24 contact, male
J78	131-0391-00	Coax, 50 Ω male
J79	131-0391-00	Coax, 50 Ω male

Connectors *(cont)*

Ckt. No.		Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
J100	*	132-0040-00			Adapter	
J114		131-0391-00			Coax, 50 Ω male	
J139		131-0391-00			Coax, 50 Ω male	
J181	*	136-0140-00			Socket, Banana Jack assembly	
J299	*	136-0140-00			Socket ,Banana Jack assembly	
J400	*	132-0040-00			Adapter	
J414		131-0391-00			Coax, 50 Ω male	
J439		131-0391-00			Coax, 50 Ω male	
J481	*	136-0140-00			Socket, Banana Jack assembly	
J599	*	136-0140-00			Socket, Banana Jack assembly	
J881		131-0206-00			Probe Power	
J882		131-0206-00			Probe Power	
Delay Line						
DL101A,B	*	119-0128-00			Delay line Assembly	
Inductors						
L20	*	120-0382-00			Toroid, 14 turns single	
L24	*	114-0179-00			500 μH 800 μH, Var Core 276-0506-00	
L71	*	108-0057-00			8.8 μH	
L77	*	120-0382-00			Toroid, 14 turns single	
L113	*	120-0382-00			Toroid, 14 turns single	
L298	*	120-0402-00			Toroid, 3 turns single	
L598	*	120-0402-00			Toroid, 3 turns single	
L751		276-0507-00	XB060000		Core, Ferramic Suppressor	
L752		276-0507-00	XB060000		Core, Ferramic Suppressor	
L753		276-0507-00	XB060000		Core, Ferramic Suppressor	
L754		276-0507-00	XB060000		Core, Ferramic Suppressor	
LR118[1]	*	308-0449-00			18 μH (1.5 kΩ)	
LR119[1]	*	308-0448-00			1.2 μH (980 Ω)	
LR418[1]	*	308-0449-00			18 μH (15 kΩ}	
LR419[1]	*	308-0448-00			1.2 μH (980 Ω)	
Transistors						
Q7		151-0179-00			Silicon	2N3877A
Q11	*	153-0556-00			Silicon	Selected 2N2501
Q31		151-0190-00			Silicon	2N3904
Q38	*	151-0133-00			Silicon	Selected from 2N3251
Q54		151-0188-00			Silicon	2N3906
Q58		151-0188-00			Silicon	2N3906
Q76	*	151-0087-00			Silicon	Replaceable by 2N1131
Q121	*	151-0198-00			Silicon	Replaceable by MPS-918
Q151		151-1012-00			Silicon	FET
Q156		151-0188-00			Silicon	2N3906
Q158		151-0188-00			Silicon	2N3906
Q170		151-0188-00			Silicon	2N3906
Q173	*	151-0192-00			Silicon	Replaceable by MPS-6521
Q201		151-0190-00			Silicon	2N3904
Q209		151-0190-00			Silicon	2N3904

[1]Coil, resistor combination.

(B)

Transistors *(cont)*

Ckt. No.		Tektronix Part No.	Serial/Model No. Eff	Disc	Description
Q221		151-0190-00		Silicon	2N3904
Q228		151-0188-00		Silicon	2N3906
Q243		151-1007-00		Silicon	Dual FET
Q244		151-0261-00	XB100000	Silicon	Dual Tek Spec
Q252		151-0188-00		Silicon	2N3906
Q261		151-0190-00		Silicon	2N3904
Q266		151-0188-00		Silicon	2N3906
Q283	*	151-0192-00		Silicon	Replaceable by MPS-6521
Q288		151-0188-00		Silicon	2N3906
Q307		151-0190-00		Silicon	2N3904
Q312		151-0188-00		Silicon	2N3906
Q421	*	151-0198-00		Silicon	Replaceable by MPS-918
Q451		151-1012-00		Silicon	FET
Q456		151-0188-00		Silicon	2N3906
Q458		151-0188-00		Silicon	2N3906
Q470		151-0188-00		Silicon	2N3906
Q473	*	151-0192-00		Silicon	Replaceable by MPS-6521
Q501		151-0190-00		Silicon	2N3904
Q509		151-0190-00		Silicon	2N3904
Q521		151-0190-00		Silicon	2N3904
Q528		151-0188-00		Silicon	2N3906
Q543		151-1007-00		Silicon	Dual FET
Q544		151-0261-00	XB100000	Silicon	Dual
Q552		151-0188-00		Silicon	2N3906
Q561		151-0190-00		Silicon	2N3904
Q566		151-0188-00		Silicon	2N3906
Q583	*	151-0192-00		Silicon	Replaceable by MPS-6521
Q588		151-0188-00		Silicon	2N3906
Q607		151-0190-00		Silicon	2N3904
Q612		151-0188-00		Silicon	2N3906
Q714		151-0188-00		Silicon	2N3906
Q724		151-0188-00		Silicon	2N3906
Q749		151-0190-00		Silicon	2N3904
Q759		151-0190-00		Silicon	2N3904
Q771	*	151-0150-01		Silicon	Selected from 2N3440
Q775	*	151-0150-01		Silicon	Selected from 2N3440
Q781	*	151-0150-01		Silicon	Selected from 2N3440
Q785		151-0150-01		Silicon	Selected from 2N3440
Q793		151-0179-00		Silicon	2N3877A
Q795		151-0179-00		Silicon	2N3877A
Q815		151-0190-00		Silicon	2N3904
Q817	*	151-0136-01		Silicon	Selected from 2N3053
Q825		151-0190-00		Silicon	2N3904
Q835		151-0190-00		Silicon	2N3904
Q839	*	151-0148-00		Silicon	Selected from 40250 (RCA)

(B)

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description	
R1	317-0510-00		51 Ω	1/8 W		5%
R3	315-0101-00		100 Ω	1/4 W		5%
R5	311-0613-00		100 kΩ, Var			
R6	315-0563-00		56 k Ω	1/4 W		5%
R9	315-0302-00		3 kΩ	1/4 W		5%
R14	315-0123-00		12 kΩ	1/4 W		5%
R22	315-0103-00		10 kΩ	1/4 W		5%
R23	315-0512-00		5.1 kΩ	1/4 W		5%
R27	315-0102-00		1 kΩ	1/4 W		5%
R29	315-0331-00		330 Ω	1/4 W		5%
R31	315-0222-00		2.2 kΩ	1/4 W		5%
R33	315-0102-00		1 kΩ	1/4 W		5%
R35	315-0512-00		5.1 kΩ	1/4 W		5%
R37	315-0363-00		36 kΩ	1/4 W		5%
R40	301-0153-00		15 kΩ	1/2 W		5%
R43	301-0153-00		15 kΩ	1/2 W		5%
R44	315-0471-00		470 Ω	1/4 W		5%
R47	317-0122-00		1.2 kΩ	1/8 W		5%
R50	315-0333-00		33 kΩ	1/4 W		5%
R52	311-0607-00		10 kΩ, Var			
R53	315-0303-00		30 kΩ	1/4 W		5%
R55	315-0103-00		10 kΩ	1/4 W		5%
R57	315-0472-00		4.7 kΩ	1/4 W		5%
R59	315-0103-00		10 kΩ	1/4 W		5%
R64	315-0301-00		300 Ω	1/4 W		5%
R65	315-0301-00		300 Ω	1/4 W		5%
R72	317-0101-00		100 Ω	1/8 W		5%
R74	308-0218-00		150 Ω	3 W	WW	5%
R76	311-0607-00		10 kΩ, Var			
R100	307-0121-00		6.757 Ω	1/10 W		1%
R101	317-0271-00		270 Ω	1/8 W		5%
R103	317-0101-00		100 Ω	1/8 W		5%
R104	317-0101-00		100 Ω	1/8 W		5%
R106	317-0101-00		100 Ω	1/8 W		5%
R107	317-0101-00		100 Ω	1/8 W		5%
R109	317-0510-00		51 Ω	1/8 W		5%
R110	317-0101-00		100 Ω	1/8 W		5%
R111	317-0101-00		100 Ω	1/8 W		5%
R112	317-0510-00		51 Ω	1/8 W		5%
R115	317-0036-00		3.6 Ω	1/8 W		5%
R116	317-0082-00		8.2 Ω	1/8 W		5%
R118	321-0097-00		100 Ω	1/8 W	Prec	1%
R119	321-0109-00		133 Ω	1/8 W	Prec	1%
R120	315-0152-00		1.5 kΩ	1/4 W		5%
R121	307-0106-00		4.7 Ω	1/4 W		5%

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc		Description	
R122	315-0621-00		620 Ω	1/4 W		5%
R124	317-0100-00		10 Ω	1/8 W		5%
R125	321-0151-00		365 Ω	1/8 W	Prec	1%
R127	315-0510-00		51 Ω	1/4 W		5%
R128	315-0272-00		2.7 kΩ	1/4 W		5%
R131	315-0470-00		47 Ω	1/4 W		5%
R132	315-0361-00		360 Ω	1/4 W		5%
R134	317-0111-00		110 Ω	1/8 W		5%
R135	317-0242-00		2.4 kΩ	1/8 W		5%
R136	317-0201-00		200 Ω	1/8 W		5%
R137	317-0201-00		200 Ω	1/8 W		5%
R138	317-0242-00		2.4 kΩ	1/8 W		5%
R139	317-0181-00		180 Ω	1/8 W		5%
R140	317-0221-00		220 Ω	1/8 W		5%
R142	321-0381-00		90.9 kΩ	1/8 W	Prec	1%
R143	321-0441-00		383 kΩ	1/8 W	Prec	1%
R144	321-0318-00		20 kΩ	1/8 W	Prec	1%
R147	315-0752-00		7.5 kΩ	1/4 W		5%
R148	308-0429-00		22 kΩ	3 W	WW	1%
R150	308-0429-00		22 kΩ	3 W	WW	1%
R151	315-0512-00		5.1 kΩ	1/4 W		5%
R152	321-0097-00		100 Ω	1/8 W	Prec	1%
R154	321-0268-00		6.04 kΩ	1/8 W	Prec	1%
R155	317-0200-00		20 Ω	1/8 W		5%
R156	317-0101-00		100 Ω	1/8 W		5%
R157	315-0123-00		12 kΩ	1/4 W		5%
R158	321-0236-00		2.8 kΩ	1/8 W	Prec	1%
R159	317-0101-00		100 Ω	1/8 W		5%
R160	317-0101-00		100 Ω	1/8 W		5%
R163	315-0332-00		3.3 kΩ	1/4 W		5%
R164	315-0132-00		13 kΩ	1/4 W		5%
R165	311-0485-00		250 Ω, Var			
R167A	321-0661-00		600 Ω	1/8 W	Prec	1%
R167B	321-0126-00		200 Ω	1/8 W	Prec	1%
R167C	321-0097-00		100 Ω	1/8 W	Prec	1%
R167D	321-0657-00		60 Ω	1/8 W	Prec	1%
R167E	321-0030-00		20 Ω	1/8 W	Prec	1%
R167F	321-0001-00		10 Ω	1/8 W	Prec	1%
R168A	321-0660-00		417 Ω	1/8 W	Prec	1%
R168B	321-0659-00		139 Ω	1/8 W	Prec	1%
R168C	321-0658-00		69.4 Ω	1/8 W	Prec	1%
R168D	321-0656-00		21.3 Ω	1/8 W	Prec	1%
R168E	321-0655-00		10.3 Ω	1/8 W	Prec	1%
R168F	321-0654-00		10.1 Ω	1/8 W	Prec	1%
R169	321-0193-00		1 kΩ	1/8 W	Prec	1%
R173	315-0114-00		110 kΩ	1/4 W		5%
R175	308-0321-00		24.4 kΩ	5 W	WW	1%

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Description		
R177	315 0102-00		1 kΩ	1/4 W		5%
R178[2]	311-0529-00		25 kΩ, Var			
R179	315-0102-00		1 kΩ	1/4 W		5%
R181	321-0289-00		10 kΩ	1/8 W	Prec	1%
R183	321-0219-02		1.87 kΩ	1/8 W	Prec	0.5%
R185	321-0744-02		20.25 kΩ	1/8 W	Prec	0.5%
R186A	321-0746-02		162.6 kΩ	1/8 W	Prec	0.5%
R186B	321-1359-02		54.2 kΩ	1/8 W	Prec	0.5%
R186C	321-1330-02		27.1 kΩ	1/8 W	Prec	0.5%
R186D	321-0743-02		16.26 kΩ	1/8 W	Prec	0.5%
R186E	321-1263-02		5420 Ω	1/8 W	Prec	0.5%
R186F	321-1234-02		2710 Ω	1/8 W	Prec	0.5%
R187	321-0197-02		1.1 kΩ	1/8 W	Prec	0.5%
R188	321-0742-02		11.84 kΩ	1/8 W	Prec	0.5%
R190	321-0441-00		383 kΩ	1/8 W	Prec	1%
R191	315-0153-00		15 kΩ	1/4 W		5%
R192	311-0510-00		10 kΩ, Var			
R193	315-0153-00		15 kΩ	1/4 W		5%
R194	321-0441-00		383 kΩ	1/8 W	Prec	1%
R196	315-0512-00		5.1 kΩ	1/4 W		5%
R197	315-0153-00		15 kΩ	1/4 W		5%
R198	311-0614-00		30 kΩ, Var			
R199	315-0512-00		5.1 kΩ	1/4 W		5%
R201	301-0563-00		56 kΩ	1/2 W		5%
R202	315-0272-00		2.7 kΩ	1/4 W		5%
R204	321-0411-00		187 kΩ	1/8 W	Prec	1%
R206	315-0303-00		30 kΩ	1/4 W		5%
R207	315-0912-00		9.1 kΩ	1/4 W		5%
R209	315-0101-00		100 Ω	1/4 W		5%
R210	315-0101-00		100 Ω	1/4 W		5%
R212	311-0614-00		30 kΩ, Var			
R213	315-0912-00		9.1 kΩ	1/4 W		5%
R215	315-0131-00		130 Ω	1/4 W		5%
R217	315-0104-00		100 kΩ	1/4 W		5%
R221	315-0101-00		100 Ω	1/4 W		5%
R223	315-0510-00		51 Ω	1/4 W		5%
R225	315-0510-00		51 Ω	1/4 W		5%
R228	315-0101-00		100 Ω	1/4 W		5%
R231	321-0235-00		2.74 kΩ	1/8 W		1%
R232	321-0231-00		2.49 kΩ	1/8 W	Prec	1%
R233	321-0231-00		2.49 kΩ	1/8 W	Prec	1%
R234	321-0235-00		2.74 kΩ	1/8 W		1%
R236	317-0242-00		2.4 kΩ	1/8 W		5%
R238	317-0242-00		2.4 kΩ	1/8 W		5%

[2]Furnished as a unit with R323.

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R243	301-0513-00			51 kΩ	1/2 W	5%
R245	315-0432-00	B100000		4.3 kΩ	1/4 W	5%
			B099999X	470 Ω	1/4 W	5%
R247	311-0635-00			1 kΩ, Var		
R249	315-0432-00	B100000		4.3 kΩ	1/4 W	5%
R251	315-0101-00			100 Ω	1/4 W	5%
R253	315-0390-00	B100000		39 Ω	1/4 W	5%
R255	315-0241-00			240 Ω	1/4 W	5%
R257	301-0513-00			51 kΩ	1/4 W	5%
R259	315-0241-40			240 Ω	1/4 W	5%
R260	315-0106-00	XB100000		10 MΩ	1/4 W	5%
R261	315-0101-00			100 Ω	1/4 W	5%
R263	317-0101-00			100 Ω	1/8 W	5%
R265	317-0101-00			100 Ω	1/8 W	5%
R267	317-0101-00			100 Ω	1/8 W	5%
R271	322-1389-01			111 kΩ	1/4 W Prec	0.5%
R272	321-0283-00			8.66 kΩ	1/8 W Prec	1%
R274	321-0292-00			10.7 kΩ	1/8 W Prec	1%
R275	322-1389-01			111 kΩ	1/4 W Prec	0.5%
R280	321-0677-00			30.4 kΩ	1/8 W Prec	0.5%
R281	321-0387-00			105 kΩ	1/8 W Prec	1%
R282	307-0006-00			68 kΩ	1/8 W	
R283	311-0607-00			10 kΩ, Var		
R284	315-0124-00			120 kΩ	1/4 W	5%
R286	315-0101-00			100 Ω	1/4 W	5%
R287	308-0320-00			15.6 kΩ	3 W WW	1%
R288	321-0677-00			30.4 kΩ	1/8 W Prec	0.5%
R289	315-0101-00			100 Ω	1/4 W	5%
R293[3]	* 311-0659-00			10 kΩ, Var		
R295	315-0102-00			1 kΩ	1/4 W	5%
R296	315-0204-00			200 kΩ	1/4 W	5%
R298	321-0745-03			25.05 kΩ	1/8 W Prec	0.25%
R299	321-1310-03			16.7 kΩ	1/8 W Prec	0.25%
R301	311-0609-00			2 kΩ, Var		
R303	315-0132-00			1.3 kΩ	1/4 W	5%
R304	321-0617-00			111 kΩ	1/8 W Prec	1%
R305	315-0681-00			680 Ω	1/4 W	5%
R307	315-0124-00			120 kΩ	1/4 W	5%
R312	308-0320-00			15.6 kΩ	3 W WW	1%
R315	315-0101-00			100 Ω	1/4 W	5%
R318	321-0309-00			16.2 kΩ	1/8 W Prec	1%
R321	321-0309-00			16.2 kΩ	1/8 W Prec	1%
R323[4]	311-0529-00			2.5 kΩ, Var		
R332	315-0203-00			20 kΩ	1/4 W	5%
R334	315-0204-00			200 kΩ	1/4 W	5%

[3]Furnished as a unit with SW293A,B.
[4]Furnished as a unit with R178.

(B)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description	
R400	307-0121-00		6.757 Ω	1/10 W		1%
R401	317-0271-00		270 Ω	1/8 W		5%
R415	317-0036-00		3.6 Ω	1/8 W		5%
R416	317-0082-00		8.2 Ω	1/8 W		5%
R418	321-0097-00		100 Ω	1/8 W	Prec	1%
R419	321-0109-00		133 Ω	1/8 W	Prec	1%
R420	315-0152-00		1.5 kΩ	1/4 W		5%
R421	307-0106-00		4.7 Ω	1/4 W		5%
R422	315-0621-00		620 Ω	1/4 W		5%
R424	317-0100-00		10 Ω	1/8 W		5%
R425	321-0151-00		365 Ω	1/8 W	Prec	1%
R427	315-0510-00		51 Ω	1/4 W		5%
R428	315-0272-00		2.7 kΩ	1/4 W		5%
R431	315-0470-00		47 Ω	1/4 W		5%
R432	315-0361-00		360 Ω	1/4 W		5%
R434	317-0111-00		110 Ω	1/8 W		5%
R435	317-0242-00		2.4 kΩ	1/8 W		5%
R436	317-0201-00		200 Ω	1/8 W		5%
R437	317-0201-00		200 Ω	1/8 W		5%
R438	317-0242-00		2.4 kΩ	1/8 W		5%
R439	317-0181-00		180 Ω	1/8 W		5%
R440	317-0221-00		220 Ω	1/8 W		5%
R442	321-0381-00		90.9 kΩ	1/8 W	Prec	1%
R443	321-0441-00		383 kΩ	1/8 W	Prec	1%
R444	321-0318-00		20 kΩ	1/8 W	Prec	1%
R447	315-0752-00		7.5 kΩ	1/4 W		5%
R448	308-0429-00		22 kΩ	3 W	WW	1%
R450	308-0429-00		22 kΩ	3 W	WW	1%
R451	315-0512-00		5.1 kΩ	1/4 W		5%
R452	321-0097-00		100 Ω	1/8 W	Prec	1%
R454	321-0268-00		6.04 kΩ	1/8 W	Prec	1%
R455	317-0200-00		20 Ω	1/8 W		5%
R456	317-0101-00		100 Ω	1/8 W		5%
R457	315-0123-00		12 kΩ	1/4 W		5%
R458	321-0236-00		2.8 kΩ	1/8 W	Prec	1%
R459	317-0101-00		100 Ω	1/8 W		5%
R460	317-0101-00		100 Ω	1/8 W		5%
R463	315-0332-00		3.3 kΩ	1/4 W		5%
R464	315-0132-00		1.3 kΩ	1/4 W		5%
R465	311-0485-00		250 Ω, Var			
R467A	321-0661-00		600 Ω	1/8 W	Prec	1%
R467B	321-0126-00		200 Ω	1/8 W	Prec	1%
R467C	321-0097-00		100 Ω	1/8 W	Prec	1%
R467D	321-0657-00		60 Ω	1/8 W	Prec	1%
R467E	321-0030-00		20 Ω	1/8 W	Prec	1%
R467F	321-0001-00		10 Ω	1/8 W	Prec	1%
R468A	321-0660-00		417 Ω	1/8 W	Prec	1%

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R468B	321-0659-00		139 Ω	1/8 W	Prec	1%
R468C	321-0658-00		69.4 Ω	1/8 W	Prec	1%
R468D	321-0656-00		21.3 Ω	1/8 W	Prec	1%
R468E	321-0655-00		10.3 Ω	1/8 W	Prec	1%
R468F	321-0654-00		10.1 Ω	1/8 W	Prec	1%
R469	321-0193-00		1 kΩ	1/8 W	Prec	1%
R473	315-0114-00		110 kΩ	1/4 W		5%
R475	308-0321-00		24.4 kΩ	5 W	WW	1%
R477	315-0102-00		1 kΩ	1/4 W		5%
R478[5]	311-0529-00		25 kΩ, Var			
R479	315-0102-00		1 kΩ	1/4 W		5%
R481	321-0289-00		10 kΩ	1/8 W	Prec	1%
R483	321-0219-02		1.87 kΩ	1/8 W	Prec	0.5%
R485	321-0744-02		20.25 kΩ	1/8 W	Prec	0.5%
R486A	321-0746-02		162.6 kΩ	1/8 W	Prec	0.5%
R486B	321-1359-02		54.2 kΩ	1/8 W	Prec	0.5%
R486C	321-1330-02		27.1 kΩ	1/8 W	Prec	0.5%
R486D	321-0743-02		16.26 kΩ	1/8 W	Prec	0.5%
R486E	321-1263-02		5420 Ω	1/8 W	Prec	0.5%
R486F	321-1234-02		2710 Ω	1/8 W	Prec	0.5%
R487	321-0197-02		1.1 kΩ	1/8 W	Prec	0.5%
R488	321-0742-02		11.84 kΩ	1/8 W	Prec	0.5%
R490	321-0441-00		383 kΩ	1/8 W	Prec	1%
R491	315-0153-00		15 kΩ	1/4 W		5%
R492	311-0510-00		10 kΩ, Var			
R493	315-0153-00		15 kΩ	1/4 W		5%
R494	321-0441-00		383 kΩ	1/8 W	Prec	1%
R496	315-0512-00		5.1 kΩ	1/4 W		5%
R497	315-0153-00		15 kΩ	1/4 W		5%
R498	311-0614-00		30 kΩ, Var			
R499	315-0512-00		5.1 kΩ	1/4 W		5%
R501	301-0563-00		56 kΩ	1/2 W		5%
R502	315-0272-00		2.7 kΩ	1/4 W		5%
R504	321-0411-00		187 kΩ	1/8 W	Prec	1%
R506	315-0303-00	B100000	30 kΩ	1/4 W		5%
R507	315-0912-00		9.1 kΩ	1/4 W		5%
R509	315-0101-00		100 Ω	1/4 W		5%
R510	315-0101-00		100 Ω	1/4W		5%
R512	311-0614-00		30 kΩ, Var			
R513	315-0912-00		9.1 kΩ	1/4 W		5%
R515	315-0131-00		130 Ω	1/4 W		5%
R517	315-0104-00		100 kΩ	1/4 W		5%
R521	315-0101-00		100 Ω	1/4 W		5%
R523	315-0510-00		51 Ω	1/4 W		5%
R525	315-0510-00		51 Ω	1/4 W		5%

[5]Furnished as a unit with R623.

(B)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Description		
R528	315-0101-00			100 Ω	1/4 W	5%
R531	321-0235-00			2.74 kΩ	1/8 W	1%
R532	321-0231-00			2.49 kΩ	1/8 W Prec	1%
R533	321-0231-00			2.49 kΩ	1/8 W Prec	1%
R534	321-0235-00			2.74 kΩ	1/8 W	1%
R536	317-0242-00			2.4 kΩ	1/8 W	5%
R538	317-0242-00			2.4 kΩ	1/8 W	5%
R543	301-0513-00			51 kΩ	1/2 W	5%
R545	315-0432-00			4.3 kΩ	1/4 W	5%
R547	311-0635-00			1 kΩ, Var		
R549	315-0432-00			4.3 kΩ	1/4 W	5%
R551	315-0101-00			100 Ω	1/4 W	5%
R553	315-0390-00			39 kΩ	1/4 W	5%
R555	315-0241-00			240 Ω	1/4 W	5%
R557	301-0513-00			51 kΩ	1/2 W	5%
R559	315-0241-00			240 Ω	1/4 W	5%
R560	315-0106-00			10 MΩ	1/4 W	5%
R561	315-0101-00			100 Ω	1/4 W	5%
R563	317-0101-00			100 Ω	1/8 W	5%
R565	317-0101-00			100 Ω	1/8 W	5%
R567	317-0101-00			100 Ω	1/8 W	5%
R571	322-1389-01			111 kΩ	1/4 W Prec	0.5%
R572	321-0283-00			8.66 kΩ	1/8 W Prec	1%
R574	321-0292-00			10.7 kΩ	1/8 W Prec	1%
R575	322-1389-01			111 kΩ	1/4 W Prec	0.5%
R580	321-0677-00			30.4 kΩ	1/8 W Prec	0.5%
R581	321-0387-00			105 kΩ	1/8 W Prec	1%
R582	307-0006-00			68 kΩ	1/8 W	
R583	311-0607-00			10 kΩ, Var		
R584	315-0124-00			120 kΩ	1/4 W	5%
R586	315-0101-00			100 Ω	1/4 W	5%
R587	308-0320-00			15.6 kΩ	3 W	1%
R588	321-0677-00			30.4 kΩ	1/8 W Prec	0.5%
R589	315-0101-00			100 Ω	1/4 W	5%
R593[6]	* 311-0659-00			10 kΩ, Var		
R595	315-0102-00			1 kΩ	1/4 W	5%
R596	315-0204-00			200 kΩ	1/4 W	5%
R598	321-0745-03			25.05 kΩ	1/8 W Prec	0.25%
R599	321-1310-03			16.7 kΩ	1/8 W Prec	0.25%
R601	311-0609-00			2 kΩ, Var		
R603	315-0132-00			1.3 kΩ	1/4 W	5%
R604	321-0617-00			111 kΩ	1/8 W Prec	1%
R605	315-0681-00			680 Ω	1/4 W	5%

[6]Furnished as a unit with SW593A,B

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R607	315-0124-00		120 kΩ	1/4 W		5%
R612	308-0320-00		15.6 kΩ	3W	WW	1%
R615	315-0101-00		100 Ω	1/4 W		5%
R618	321-0309-00		16.2 kΩ	1/8 W	Prec	1%
R621	321-0309-00		16.2 kΩ	1/8 W	Prec	1%
R623[7]	311-0529-00		2.5 kΩ, Var			
R641	321-1289-01		10.1 kΩ	1/8 W	Prec	0.5%
R701	315-0203-00		20 kΩ	1/4 W		5%
R703	315-0100-00		10 Ω	1/4 W		5%
R707	315-0222-00		2.2 kΩ	1/4 W		5%
R708	315-0223-00		22 kΩ	1/4 W		5%
R709	315-0103-00		10 kΩ	1/4 W		5%
R711	315-0101-00		100 Ω	1/4 W		5%
R713	315-0101-00		100 Ω	1/4 W		5%
R715	315-0562-00		5.6 kΩ	1/4 W		5%
R718	315-0105-00		1 MΩ	1/4 W		5%
R719	315-0363-00		36 kΩ	1/4 W		5%
R723	315-0101-00		100 Ω	1/4 W		5%
R725	315-0562-00		5.6 kΩ	1/4 W		5%
R728	315-0105-00		1 MΩ	1/4 W		5%
R729	315-0363-00		36 kΩ	1/4 W		5%
R748	321-0295-00		11.5 kΩ	1/8 W	Prec	1%
R749	321-0250-00		3.92 kΩ	1/8 W	Prec	1%
R753	321-0238-00		2.94 kΩ	1/8 W	Prec	1%
R756	311-0635-00		1 kΩ, Var			
R758	321-0293-00		11 kΩ	1/8 W	Prec	1%
R759	321-0250-00		3.92 kΩ	1/8 W	Prec	1%
R762	321-0231-00		2.49 kΩ	1/8 W	Prec	1%
R764	311-0091-00		1 kΩ, Var			
R766	311-0607-00		10 kΩ, Var			
R767	315-0333-00		33 kΩ	1/4 W		5%
R769	315-0223-00		22 kΩ	1/4 W		5%
R771	301-0303-00		30 kΩ	1/2 W		5%
R772	301-0303-00		30 kΩ	1/2 W		5%
R777	323-0405-00		162 kΩ	1/2 W	Prec	1%
R779	301-0164-00		160 kΩ	1/2 W		5%
R780	321-0284-00		8.87 kΩ	1/8 W	Prec	1%
R781	301-0303-00		30 kΩ	1/2 W		5%
R782	301-0303-00		30 kΩ	1/2 W		5%
R787	301-0164-00		160 kΩ	1/2 W		5%
R789	301-0164-00		160 kΩ	1/2 W		5%
R791	315-0304-00		300 kΩ	1/4 W		5%
R793	315-0304-00		300 kΩ	1/4 W		5%
R795	315-0624-00		620 kΩ	1/4 W		5%
R797	315-0106-00		10 MΩ	1/4 W		5%

[7]Furnished as a unit with R478.

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc				
R801	301-0473-00			47 kΩ	1/2 W		5%
R803	315-0102-00			1 kΩ	1/4 W		5%
R813	321-0311-00			16.9 kΩ	1/8 W	Prec	1%
R814	322-0367-00			64.9 kΩ	1/4 W	Prec	1%
R815	315-0102-00			1 kΩ	1/4 W		5%
R817	308-0299-00			300 Ω	3 W	WW	1%
R825	315-0114-00			110 kΩ	1/4 W		5%
R827	315-0182-00			1.8 kΩ	1/4 W		5%
R829	315-0124-00			120 kΩ	1/4 W		5%
R831	321-0193-00			1 kΩ	1/8 W	Prec	1%
R832	311-0605-00			200 Ω, Var			
R833	321-0172-00			604 Ω	1/8 W	Prec	1%
R835	315-0123-00			12 kΩ	1/4 W		5%
R841	308-0293-00	B010100	B030600X	4 kΩ	3 W	WW	5%
R843	308-0293-00			4 kΩ	3 W	WW	5%
R851	315-0101-00			100 Ω	1/4 W		5%
R853	315-0101-00			100 Ω	1/4 W		5%
R861	315-0101-00			100 Ω	1/4 W		5%
R863	315-0101-00			100 Ω	1/4 W		5%
R865	315-0101-00			100 Ω	1/4 W		5%
R867	315-0101-00			100 Ω	1/4 W		5%

Switches

	Unwired or Wired				
SW110A, SW110B	wired *	262-0811-00	Rotary		INTERNAL TRIGGER SAMPLING MODE
SW110A, SW110B		260-0857-00	Rotary		INTERNAL TRIGGER SAMPLING MODE
SW168	wired *	262-0810-00	Rotary		CH A VOLTS/DIV
SW168		260-0859-00	Rotary		CH A VOLTS/DIV
SW290		260-0816-00	Slide		CH A INVERT NORM
SW293A,B[8]		311-0659-00			CH A CAL
SW468	wired *	262-0810-00	Rotary		CH B VOLTS/DIV
SW468		260-0859-00	Rotary		CH B VOLTS/DIV
SW590		260-0816-00	Slide		CH B INVERT NORM
SW593A,B[9]	*	311-0659-00			CH B CAL
SW730A, SW730B	wired *	262-0812-00	Rotary		VERTICAL MODE

[8]Furnished as a unit with R293.

[9]Furnished as a unit with R593.

Switches *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SW730A SW730B	260-0858-00		Rotary	VERTICAL MODE

Transformers

T12	* 120-0511-00		Toroid, 2 turns-12 turns
T72	* 120-0491-00		Toroid, 7 turns bifilar
T113	276-0554-00		Core, Toroid Ferrite
T139	* 120-0490-01		Toroid, 5 turns (twisted pair)
T140	* 120-0512-00		Toroid, 5 turns
T235	* 120-0492-00		Toroid, 3 windings
T439	* 120-0490-01		Toroid, 5 turns (twisted pair)
T440	* 120-0512-00		Toroid, 5 turns
T535	* 120-0492-00		Toroid, 5 turns bifilar
T820	* 120-0488-00		Power

Test Points

TP38	* 214-0579-00		Pin, Test Point
TP58	* 214-0579-00		Pin, Test Point
TP161	* 214-0579-00		Pin, Test Point
TP196	* 214-0579-00		Pin, Test Point
TP199	* 214-0579-00		Pin, Test Point
TP229	* 214-0579-00		Pin, Test Point
TP235	* 214-0579-00		Pin, Test Point
TP279	* 214-0579-00		Pin, Test Point
TP288	* 214-0579-00		Pin, Test Point
TP313	* 214-0579-00		Pin, Test Point
TP461	* 214-0579-00		Pin, Test Point
TP496	* 214-0579-00		Pin, Test Point
TP499	* 214-0579-00		Pin, Test Point
TP529	* 214-0579-00		Pin, Test Point
TP535	* 214-0579-00		Pin, Test Point
TP579	* 214-0579-00		Pin, Test Point
TP588	* 214-0579-00		Pin, Test Point
TP613	* 214-0579-00		Pin, Test Point
TP707	* 214-0579-00		Pin, Test Point
TP714	* 214-0579-00		Pin, Test Point
TP724	* 214-0579-00		Pin, Test Point
TP817	* 214-0579-00		Pin, Test Point
TP838	* 214-0579-00		Pin, Test Point
TP839	* 214-0579-00		Pin, Test Point

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations which appear either on the back of the diagrams or on pullout pages immediately following the diagrams of the instruction manual.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the Description column.

Assembly and/or Component
Detail Part of Assembly and/or Component mounting hardware for Detail Part
Parts of Detail Part mounting hardware for Parts of Detail Part
mounting hardware for Assembly and/or Component

Mounting hardware always appears in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Mounting hardware must be purchased separately, unless otherwise specified.

PARTS ORDERING INFORMATION

See parts ordering information on page preceding page 9-1.

ABBREVIATIONS AND SYMBOLS

For an explanation of the abbreviations and symbols used in this section, please refer to the page immediately preceding the Electrical Parts List in this instruction manual.

INDEX OF MECHANICAL PARTS UST ILLUSTRATIONS

(Located behind diagrams)

SECTION 10
MECHANICAL PARTS LIST

FIG. 1 FRONT

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
1-1	366-0319-00			1	KNOB, red - DC OFFSET (CHANNEL A)
	- - - - - - - - - -			-	knob includes:
	213-0020-00			1	SCREW, set, 6-32 x 1/8 inch, HSS
-2	366-0408-00			1	KNOB, charcoal - A POSITION
	- - - - - - - - - -			-	knob includes:
	213-0048-00			1	SCREW, set, 4-40 x1/8 inch, HSS
-3	- - - - - - - - - -			1	RESISTOR, variable
	- - - - - - - - - -			-	mounting hardware: (not included w/resistor)
-4	210-0207-00			1	LUG, solder, 3/8 ID x 5/8 inch OD, SE
-5	210-0012-00			1	LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
-6	210-0978-00			1	WASHER, flat, 3/8 ID x 1/2 inch OD
-7	210-0590-00			1	NUT, hex., 3/8-32x 7/16 inch
-8	366-0189-00			1	KNOB, red - SMOOTH NORMAL
	- - - - - - - - - -			-	knob includes:
	213-0020-00			1	SCREW, set 6-32 x 1/8 inch, HSS
-9	366-0322-00			1	KNOB, charcoal-DUAL TRACE
	- - - - - - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-10	262-0812-00			1	SWITCH, wired-DUAL TRACE
	- - - - - - - - - -			-	switch includes:
	260-0858-00			1	SWITCH, unwired
	- - - - - - - - - -			-	mounting hardware: (not included w/switch)
-11	210-0590-00			1	NUT, hex., 3/8-32x 7/16 inch
-12	366-0319-00			1	KNOB, red - DC OFFSET (CHANNEL B)
	- - - - - - - - - -			-	knob includes:
	213-0020-00			1	SCREW, set, 6-32 x 1/8 inch, HSS
-13	366-0408-00			1	KNOB, charcoal - B POSITION
	- - - - - - - - - -			-	knob includes.
	213-0048-00			1	SCREW, set, 4-40 x 1/8 inch, HSS
-14	- - - - - - - - - -			1	RESISTOR, variable
	- - - - - - - - - -			-	mounting hardware: (not included w/resistor)
-15	210-0207-00			1	LUG, solder, 3/8 ID x 5/8 inch OD, SE
-16	210-0012-00			1	LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
-17	210-0978-00			1	WASHER, flat, 3/8 ID x 1/2 inch OD
-18	210-0590-00			1	NUT, hex., 3/8-32x 7/16 inch

Ⓐ

FIG. 1 FRONT *(cont)*

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
1-19	366-0189-00			1	KNOB, red - CAL (CHANNEL A) knob includes:
	- - - - - - - - - -			-	knob includes:
	213-0020-00			1	SCREW, set, 6-32 x 1/8 inch, HSS
-20	366-0322-00			1	KNOB, charcoal - mVOLTS/DIV (CHANNEL A)
	- - - - - - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-21	262-0810-00			1	SWITCH, wired - mVOLTS/DIV (CHANNEL A)
	- - - - - - - - - -			-	switch includes:
	260-0859-00			1	SWITCH, unwired
-22	384-0671-00			1	SHAFT, extension
-23	- - - - - - - - - -			1	RESISTOR, variable
	- - - - - - - - - -			-	mounting hardware: (not included w/resistor)
-24	211-0114-00			2	SCREW, 4-40 x 1/2 inch, PHS
-25	361-0154-00			2	SPACER, sleeve, 0.188 inch long
	- - - - - - - - - -			-	mounting hardware: (not included w/switch)
-26	210-0255-00			1	LUG, solder, 3/8 inch ID
-27	210-0590-00			1	NUT, hex, 3/8-32 x 7/16 inch
-28	366-0189-00			1	KNOB, red - CAL (CHANNEL B)
	- - - - - - - - - -			-	knob includes:
	213-0020-00			1	SCREW, set, 6-32 x 1/8 inch, HSS
-29	366-0322-00			1	KNOB, charcoal - mVOLTS/DIV (CHANNEL B)
	- - - - - - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set 6-32 x 3/16 inch, HSS
-30	262-0810-00			1	SWITCH, wired - mVOLTS/DIV (CHANNEL B)
	- - - - - - - - - -			-	switch includes:
	260-0859-00			1	SWITCH, unwired
-31	384-0671-00			1	SHAFT, extension
-32	- - - - - - - - - -			1	RESISTOR, variable
	- - - - - - - - - -			-	mounting hardware: (not included w/resistor)
-33	211-0014-00			2	SCREW, 4-40 x 1/2 inch, PHS
-34	361-0154-00			2	SPACER, sleeve, 0.188 inch long
	- - - - - - - - - -			-	mounting hardware: (not included w/switch)
-35	210-0255-00			1	LUG, solder, 3/8 inch ID
-36	210-0590-00			1	NUT, hex., 3/8-32 x 7/16 inch
-37	366-0140-00			1	KNOB, red - SAMPLING MODE
	- - - - - - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-38	366-0254-00			1	KNOB, charcoal - INTERNAL TRIGGER
	- - - - - - - - - -			-	knob includes:
	213-0020-00			1	SCREW, set, 6-32 x 1/8 inch, HSS
-39	262-0811-00			1	SWITCH, wired - INTERNAL TRIGGER
	- - - - - - - - - -			-	switch includes:
	260-0857-00			1	SWITCH, unwired
-40	175-0453-00			2	ASSEMBLY, cable
	- - - - - - - - - -			-	each assembly includes:
	- - - - - - - - - -			1	CONNECTOR, right angle, female
	- - - - - - - - - -			-	mounting hardware: (not included w/switch)
-41	210-0978-00			1	WASHER, flat, 3/8 ID x 1/2 inch OD
-42	210-0590-00			1	NUT, hex., 3/8-32 x 7/16 inch

FIG. 1 FRONT *(cont)*

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
1-43	366-0109-00			1	KNOB, plug-in securing
	- - - - - - - - - -			-	knob includes:
	213-0005-00			1	SCREW, set, 8-32 x 1/8 inch, HSS
-44	214-0052-00			1	FASTENER, pawl right
	- - - - - - - - - -			-	mounting hardware: (not included w/fastener)
	210-0004-00			1	LOCKWASHER, internal #4 (not shown)
-45	210-0406-00			2	NUT, hex., 4-40 x 3/16 inch
-46	136-0140-00			4	SOCKET, banana jack
	- - - - - - - - - -			-	mounting hardware for each: (not included w/socket)
-47	210-0895-00			1	WASHER, plastic insulating
	210-0583-00			2	NUT, hex., 1/4-32 x 5/16, inch
	210-0269-00			1	LUG, solder, terminal
-48	358-0054-00			2	BUSHING
-49	- - - - - - - - - -			2	RESISTOR, variable
	- - - - - - - - - -			-	mounting hardware for each: (not included w/resistor)
-50	210-0223-00			1	LUG, solder, 1/4 ID x 7/16 inch OD, SE
-51	210-0471-00			1	NUT, hex., 1/4-32 x 5/16 x 19/32 inch long
-52	358-0054-00			1	BUSHING
-53	- - - - - - - - - -			1	RESISTOR, variable
	- - - - - - - - - -			-	mounting hardware: (not included w/resistor)
	210-0046-00			1	LOCKWASHER, internal, 1/4 ID x 0.400 inch OD
-54	210-0471-00			1	NUT, hex., 1/4-32 x 5/16 x 19/32 inch long
-55	131-0206-00			2	CONNECTOR, probe power, 4 pin
	- - - - - - - - - -			-	mounting hardware for each: (not included w/connector)
-56	210-0270-00			1	LUG, solder, terminal
	210-0941-00	XB020550		1	WASHER, flat 0.448 ID x 11/16 inch OD (not shown)
-57	210-0559-00			1	NUT, hex., 7/16-28 x 9/16 inch
-58	352-0084-00			4	HOLDER, neon, single
-59	378-0541-00			4	FILTER, lens, neon
-60	200-0609-00			4	COVER, neon holder
-61	132-0040-00			2	ADAPTER, panel
	- - - - - - - - - -			-	mounting hardware for each: (not included w/adapter)
-62	211-0101-00			4	SCREW, 4-40 x 1/4 inch, 100° csk, FHS

(B)

FIG. 1 FRONT *(cont)*

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5 Description
1-63	260-0816-00			1	SWITCH, slide - INVERT NORM (CHANNEL A)
	- - - - - - - - - -			-	mounting hardware: (not included w/switch)
-64	211-0030-00			2	SCREW, 2-56 x 1/4 inch, FHS
-65	210-0405-00			2	NUT, hex., 2-56 x 3/16 inch
-66	260-0816-00			1	SWITCH, slide-INVERT NORM (CHANNEL B)
	- - - - - - - - - -			-	mounting hardware: (not included w/switch)
	211-0030-00			2	SCREW, 2-56 x 1/4 inch, FHS (not shown)
-67	210-0405-00			2	NUT, hex., 2-56 x 3/16 inch
-68	333-0978-01	B010100	B049999	1	PANEL, front
	333-0978-03	B050000		1	PANEL, front
-69	386-1189-00			1	PLATE, sub-panel
-70	200-0263-00	XB030680		2	COVER, plastic, variable resistor

FIG. 2 DELAY-LINE ASSEMBLY

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
2-	119-0128-00			1	ASSEMBLY, delay-line
	- - - - - - - - - -			-	assembly includes:
-1	380-0118-00			2	HOUSING
-2	129-0116-00			4	POST, 2.828 inches long
-3	200-0735-00			1	COVER, top
-4	200-0736-00			1	COVER, bottom
-5	211-0510-00			8	SCREW, 6-32 x 3/8 inch, PHS
-6	210-0949-00			4	WASHER, flat, 9/64 ID x 1/2 inch OD
-7	361-0161-00			1	SPACER, plate
-8	132-0016-00			2	NUT, retaining
-9	132-0131-00			2	SHELL
-10	132-0001-00			2	NUT, coupling
-11	132-0007-00			2	RING, snap
-12	214-0871-00			2	CONTACT, electrical
-13	132-0028-00			2	INSULATOR, plastic
-14	132-0029-00			2	CONDUCTOR, inner
-15	132-0002-00			2	SLEEVE, outer conductor
-16	220-0470-00			2	NUT, coupling
-17	210-0917-00			2	WASHER, plastic, 0.191 ID x 5/8 inch OD
-18	166-0440-00			2	FERRULE
-19	354-0304-00			2	RING, rubber
-20	166-0441-00			2	FERRULE
-21	214-0870-00			2	SPRING, ground
-22	132-0129-01			2	DIELECTRIC
-23	132-0129-02			2	DIELECTRIC
-24	361-0150-00			2	CONNECTOR, receptacle, coaxial
-25	131-0515-00			2	CONTACT, electric
	- - - - - - - - - -			-	mounting hardware: (not included w/assembly)
-26	211-0507-00			4	SCREW, 6-32 x 5/16 inch, PHS
	210-0457-00			2	NUT, keps, 6-32 x 5/16 inch (not shown)
-27	210-0803-00			2	WASHER, flat, 0.150 ID x 3/8 inch OD

(B)

Mechanical Parts List - Type 3S1

FIG. 3 CHASSIS & REAR

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
3-1	386-1190-00			1	PLATE, chassis support
	- - - - - - - - - -			-	plate includes:
-2	211-0094-00			4	SCREW, 4-40 x 1/2 inch, PHS
-3	- - - - - - - - - -			1	TRANSISTOR
	- - - - - - - - - -			-	mounting hardware: (not included w/transistor)
-4	211-0510-00			2	SCREW, 6-32 x 3/8 inch, PHS
-5	210-0202-00			1	LUG, solder, SE #6
-6	386-0143-00			1	PLATE insulator
-7	210-0935-00			2	WASHER, fiber, 0.140 ID x 0.375 inch OD
-8	210-0803-00			2	WASHER, flat, 0.150 ID x 3/8 inch OD
-9	210-0457-00			2	NUT, keps, 6-32 x 5/16 inch
-10	210-0201-00			1	LUG, solder, SE #4
	- - - - - - - - - -			-	mounting hardware: (not included w/lug)
-11	213-0044-00			1	SCREW, thread forming, 5-32 x 3/16 inch, PHS
-12	344-0117-00			1	CLIP, capacitor mounting
	- - - - - - - - - -			-	mounting hardware: (not included w/clip)
-13	213-0044-00			1	SCREW, thread forming, 5-32 x 3/16 inch, PHS
-14	407-0324-00			1	BRACKET, transformer
	- - - - - - - - - -			-	mounting hardware (not included w/bracket)
-15	210-0201-00			1	LUG, solder, SE #4
-16	213-0138-00	B010100	B020479	3	SCREW, sheet metal, #4 x 3/16 inch, PHS
	213-0138-00	B020480		2	SCREW, sheet metal, #4 x 3/16 inch, PHS
	213-0088-00	B020480		1	SCREW, thread forming, #4 x 1/4 inch, PHS
-17	358-0215-00			2	BUSHING, plastic
-18	441-0721-00			1	CHASSIS, Channel A
	- - - - - - - - - -			-	mounting hardware: (not included w/chassis)
-19	210-0457-00			2	NUT, keps, 6-32 x 5/16 inch
-20	211-0504-00			3	SCREW, 6-32 x 1/4 inch, PHS
-21	343-0089-00			1	CLAMP, cable, plastic
-22	670-0146-00			1	ASSEMBLY, circuit board-CHANNEL A
	- - - - - - - - - -			-	assembly includes:
	388-0846-00			1	BOARD, circuit
-23	214-0506-00			42	PIN, connector
-24	214-0579-00			12	PIN, test point
-25	136-0220-00			18	SOCKET, transistor, 3 pin
-26	344-0108-00			8	CLIP, diode
-27352-0101-00				1	HOLDER, toroid
	- - - - - - - - - -			-	mounting hardware: (not included w/holder)
-28	361-0008-00			1	SPACER, plastic, 5/32 inch long

FIG. 3 CHASSIS & REAR *(cont)*

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
3-29	352-0100-00			1	HOLDER, variable resistor
	- - - - - - - - - -			-	mounting hardware: (not included w/holder)
-30	361-0008-00			1	SPACER, plastic, 5/32 inch long
-31	131-0391-00			2	CONNECTOR, coaxial, 1 contact, male
-32	337-0938-00			1	SHIELD, electrical
-33	136-0234-00			4	RECEPTACLE
-34	337-0940-00			1	SHIELD, electrical
-35	136-0219-00			1	SOCKET, transistor, 4 pin
-36	136-0235-00			1	SOCKET, transistor, 6 pin
	- - - - - - - - - -			-	mounting hardware: (not included w/assembly)
-37	211-0116-00			6	SCREW, sems, 4-40 x 5/16 inch, PHB
-38	441-0720-00			1	CHASSIS, Channel B
	- - - - - - - - - -			-	mounting hardware: (not included w/chassis)
	210-0457-00			2	NUT, keps, 6-32 x 5/16 inch
-39	211-0504-00			3	SCREW, 6-32 x 5/16 inch, PHS
-40	670-0147-00			1	ASSEMBLY, circuit board-CHANNEL B
	- - - - - - - - - -			-	assembly includes:
	388-0847-00			1	BOARD, circuit
-41	214-0506-00			39	PIN, connector
-42	214-0579-00			11	PIN, test point
-43	136-0220-00			17	SOCKET, transistor, 3 pin
-44	131-0391-00			2	CONNECTOR, coaxial, 1 contact male
-45	352-0101-00			1	HOLDER, toroid
	- - - - - - - - - -			-	mounting hardware: (not included w/holder)
-46	361-0008-00			1	SPACER, plastic, 5/32 inch long
-47	352-0100-00			1	HOLDER, variable resistor
	- - - - - - - - - -			-	mounting hardware: (not included w/holder)
-48	361-0008-00			1	SPACE, plastic, 5/32 inch long
-49	344-0108-00			8	CLIP, diode
-50	136-0235-00			1	SOCKET, transistor, 6 pin
-51	337-0937-00			1	SHIELD, electrical
-52	136-0234-00			4	RECEPTACLE
-53	337-0941-00			1	SHIELD, electrical
-54	136-0219-00			1	SOCKET, transistor, 4 pin
-55	136-0183-00			1	SOCKET, transistor, 3 pin
-56	200-0385-00			1	COVER, transistor
	- - - - - - - - - -			-	mounting hardware: (not included w/assembly]
-57	211-0116-00			6	SCREW, sems, 4-40 x 5/16 inch, PHB

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FIG. 3 CHASSIS & REAR *(cont)*

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
3-58	670-0148-00			1	ASSEMBLY, circuit board-STROBE
	- - - - - - - - - -			-	assembly includes:
	388-0848-00			1	BOARD, circuit
-59	337-0939-00			1	SHIELD, electrical
-60	136-0234-00			4	RECEPTACLE
-61	337-0936-00			1	SHIELD, electrical
-62	131-0391-00			3	CONNECTOR, coaxial, 1 contact, male
-63	352-0100-00			5	HOLDER variable resistor
	- - - - - - - - - -			-	mounting hardware for each: (not included w/holder)
-64	361-0007-00			1	SPACER, plastic, 0.062 inch long
-65	214-0579-00			6	PIN, test point
-66	136-0220-00			11	SOCKET, transistor, 3 pin
-67	136-0183-00			5	SOCKET, transistor, 3 pin
-68	200-0385-00			1	COVER, transistor, 1/16 inch long
-69	344-0061-00			2	CLIP, diode
	136-0252-00	B010100	B080969	3	SOCKET, pin connector
	136-0252-01	B080970		3	SOCKET, pin connector
-70	213-0172-00			1	SCREW, thumb
	354-0311-00			1	RING, rubber
-71	407-0356-00			2	BRACKET, circuit board mounting
	- - - - - - - - - -			-	mounting hardware for each: (not included w/bracket)
-72	213-0088-00			2	SCREW, thread forming, #4 x 1/4 inch, PHS
-73	175-0414-01	B010100	B060789	2	CABLE ASSEMBLY
	175-0414-00	B060790		2	CABLE ASSEMBLY
	- - - - - - - - - -			-	each cable assembly includes:
	- - - - - - - - - -			2	CONNECTOR, right angle, female
-74	179-1191-00			1	CABLE HARNESS, A Chassis
	- - - - - - - - - -			-	cable harness includes:
	131-0371-00			29	CONNECTOR, single contact
-75	179-1192-00			1	CABLE HARNESS, B Chassis
	- - - - - - - - - -			-	cable harness includes
	131-0371-00			53	CONNECTOR, single contact
-76	179-1193-00			1	CABLE HARNESS, switch
-77	131-0149-00			1	CONNECTOR, 24 contact
	- - - - - - - - - -			-	mounting hardware: (not included w/connector)
-78	211-0016-00			2	SCREW, 4-40 x 5/8 inch, RHS
-79	166-0032-00			2	SPACER
	210-0201-00			1	LUG, solder, SE #4 (not shown)
-80	210-0586-00			2	NUT, keps, 4-40 x 1/4 inch

FIG. 3 CHASSIS & REAR *(cont)*

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description 1 2 3 4 5
3-81	351-0037-00			1	GUIDE, shoe
	- - - - - - - - - -			-	mounting hardware: (not included w/guide)
-82	211-0013-00			1	SCREW, 4-40 x 3/8 inch, RHS
-83	210-0586-00			1	NUT, keps, 4-40 x 1/4 inch
-84	131-0149-00			1	CONNECTOR, 24 contact
	- - - - - - - - - -			-	mounting hardware: (not included w/connector)
-85	211-0008-00			2	SCREW, 4-40 x 1/4 inch, PHS
-86	210-0586-00			2	NUT, keps, 4-40 x 1/4 inch
-87	210-0202-00			1	LUG, solder, SE #6
	- - - - - - - - - -			-	mounting hardware: (not included w/lug)
-88	211-0507-00			1	SCREW, 6-32 x 5/16, inch, PHS
-89	210-0457-00			1	NUT, keps, 6-32 x 5/16 inch
-90	384-0615-00			4	ROD, spacer
	- - - - - - - - - -			-	mounting hardware for each: (not included w/rod)
-91	212-0044-00			1	SCREW, 8-32 x 1/2 inch, RHS
-92	387-0595-00			1	PLATE, rear

SECTION 12

PREVENTIVE MAINTENANCE INSTRUCTIONS

12.1 SCOPE OF MAINTENANCE

The maintenance duties assigned to the operator and organizational repairman of this equipment are listed below with a reference to the paragraphs covering the specific maintenance functions. The preventive maintenance procedures require no special tools or test equipment.

a. Daily preventive maintenance checks and services (paragraph 12.5).

b. Weekly preventive maintenance checks and services (paragraph 12.6).

c. Monthly preventive maintenance checks and services (paragraph 12.7).

d. Quarterly preventive maintenance checks and services (paragraph 12.9).

e. Cleaning (paragraph 12.11).

f. Touchup painting instructions (paragraph 12.12).

12.2 MATERIALS REQUIRED FOR MAINTENANCE

a. Trichloroethane (Federal Stock No. 6810-292-9625).

WARNING

The fumes of trichloroethane are toxic. Provide thorough ventilation whenever used. DO NOT use near an open flame. Trichloroethane is not flammable, but exposure of the fumes to an open flame converts the fumes to highly toxic, dangerous gases.

b. Cleaning cloth.

c. Fine sandpaper.

d. Touchup paint.

12.3 PREVENTIVE MAINTENANCE

Preventive maintenance is the systematic care, servicing, and inspection of equipment to prevent the occurrence of trouble to reduce downtime and to assure that the equipment is serviceable.

a. Systematic Care. The procedure given in paragraphs 12.3 through 12.12 covers routine systematic care and cleaning essential to proper upkeep and operation of the equipment.

b. Preventive Maintenance Checks and Services. The maintenance checks and services charts outline functions to be performed at specific intervals. These checks and services are to maintain equipment in a combat serviceable condition; that is, in good operating condition. To assist operators in maintaining combat serviceability, the charts indicate what to check, how to check, and the normal conditions. The reference column lists the paragraphs that contain additional information. If the defect cannot be found by performing the corrective action indicated higher category of maintenance or repair is required. Records and reports of these checks and services must be made in accordance with the requirements set forth in TM 38-750.

12.4 PREVENTIVE MAINTENANCE CHECKS AND SERVICES PERIODS

Preventive maintenance checks and services of this equipment are required weekly, monthly, and quarterly. Daily maintenance checks and services are specified in paragraph 12.5. Paragraph 12.6 specifies checks and services that must be performed weekly. If the equipment is maintained in a standby condition, the daily and weekly checks should be accomplished at the same time. The maintenance checks and services that are accomplished monthly are specified in paragraph 12.7. Quarterly maintenance checks and services are specified in paragraph 12.9.

12.5 DAILY PREVENTIVE MAINTENANCE CHECKS AND SERVICES CHART

Sequence No.	Items to be inspected	Procedure	Reference
1	Completeness	See that the equipment is complete.	Appendix B
2	Cleanliness	Exterior of equipment must be clean and dry, free of fungus, dirt, dust or grease.	Paragraph 12.11
3	Operational Check	Check the operational efficiency.	
4	Controls	See that controls operate smoothly and are fastened in place securely.	

12.6 WEEKLY PREVENTIVE MAINTENANCE AND SERVICES CHART

Sequence No.	Items to be inspected	Procedure	Reference
1	Components	Inspect cards and cables for chafed, cracked, or frayed insulation. Replace connectors that are broken, stripped, or worn.	
2	Metal surfaces	Inspection exposed metal surface for rust and corrosion. Clean and touch with paint as required.	Paragraphs 12.11 and 12.12.

12.7 MONTHLY MAINTENANCE

Perform the maintenance functions indicated in the monthly preventive maintenance checks and services chart (paragraph 12.8) once each month. Periodic daily (paragraph 12.5) and weekly (paragraph 12.6) services constitute a part of the monthly checks.

12.8 MONTHLY PREVENTIVE MAINTENANCE CHECKS AND SERVICES CHART

Sequence No.	Item to be inspected	Procedure
1	Terminations	Inspect for loose connections and cracked or broken insulation.
2	Control panel	Clean panel thoroughly and check all surfaces for chips, cracks, or abnormal wear.
3	Hardware	Inspect all hardware for possible damage.

12.9 QUARTERLY MAINTENANCE

Quarterly preventive maintenance checks and services are required for this equipment. Periodic daily, weekly, and monthly services constitute a part of the quarterly preventive maintenance checks and services and must be performed concurrently. All deficiencies or shortcomings will be recorded in accordance with the requirements of TM 38-750. Perform all the checks and services listed in the quarterly preventive maintenance checks and services chart (paragraph 12.10) in the sequence listed. Adjustment of the maintenance interval must be made to compensate for any unusual operating conditions.

12.10 QUARTERLY PREVENTIVE MAINTENANCE CHECKS AND SERVICES CHART

Sequence No.	Items to be inspected	Procedure	Reference
1	Publications	See that all publications are complete, serviceable, and current.	DA Pam 310-4
2	Modifications	Check DA Pam 310-7 to determine whether new applicable MWO's have been published. All URGENT MWO's must be applied immediately. ALL NORMAL MWO's must be scheduled.	TM 38-750 and DA Pam 310-7

12.11 CLEANING

Inspect the exterior surfaces. The surfaces must be free of dust, dirt, grease, and fungus.

a. Remove dust and loose dirt with a clean, soft cloth.

b. Remove grease, fungus, and ground-in dirt. Use a damp cloth (not wet) with trichloroethane to clean terminations. If dirt on the body of the unit is difficult to remove, use mild soap and water.

c. Remove dust or dirt from the jacks and plugs with a brush.

12.12 TOUCHUP PAINTING INSTRUCTIONS

Remove dust and corrosion from metal surfaces by lightly sanding them with fine sandpaper. Brush two thin coats of paint on the bare metal to protect it from further corrosion. Refer to applicable cleaning and refinishing practices specified in TB 746-10.

APPENDIX A

REFERENCES

Following is a list of publications available to the Dual Trace Sampling Unit, Tektronix Type 351 operator and maintenance personnel.

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 7, 8, and 9), Supply Bulletins and Lubrication Orders.
DA Pam 310-7	U. S. Army Equipment Index of Modification Work Orders.
TM 38-750	The Army Maintenance Management System (TAMMS).
SB 38-100	Preservation, Packaging, Packing, and Marking Materiels, Supplies, and Equipment used by the Army.
TB 746-10	Field Instruction for Painting and Preserving Electronic Equipment.
TB 750-236	Calibration Requirements for the Maintenance of Army Materiel.

APPENDIX B

BASIS ISSUE ITEMS LIST, AND

ITEMS TROOP INSTALLED OR AUTHORIZED LIST

Effective Date: 1 July 1973

SECTION 1

INTRODUCTION

B-1 SCOPE

B-1.1 This appendix lists items which accompany the Dual Trace Sampling Unit, Tektronix Type 3S1 and are required for installation, operation, or maintenance

B-2 GENERAL

B-2.1 The Basic Issue Items List and Items Troop Installed or Authorized List are divided into the following sections.

a. Basic Issue Items - Section 2. A list of items which accompany Dual Trace Sampling Unit, Tektronix Type 3S1 and are required by the operator/crew for installation, operation, or maintenance.

b. Items Troop Installed or Authorized List - Section 3. Not applicable.

c. Maintenance and Operating Supplies - Section 4. Not applicable.

Section II. BASIC ISSUE ITEMS LIST

(1) SMR CODE	(2) FEDERAL STOCK NUMBER	(3) DESCRIPTION *References Number & Mfr. Code* *Usable On Code*	(4) UNIT OF MEAS	(5) QTY FURN WITH EQUIP	(6) ILLUSTRATION (a) FIGURE NO.	(6) ILLUSTRATION (b) ITEM NO.
		CABLE, 50 Ω, 5 Nsec B010100 to B04999 - 017-0502-00	2 ea			
		CABLE, 50 Ω, 5 Nsec B050000 up 017-0512-00	2 ea			
		ATTENUATOR, 50 Ω, 10X B05000 up 017-0078-00	2 ea			

APPENDIX C

MAINTENANCE ALLOCATION CHART

MAINTENANCE ALLOCATION CHART	Date: 1 June 1972

Nomenclature of End Item or Component:
DUAL TRACE SAMPLING UNIT, 7910657-1

This Maintenance Allocation Chart designates overall responsibility for the performance of maintenance functions on the identified end item or component. The implementation of field maintenance tasks upon this end item or component will be consistent with the assigned maintenance operations which are defined as follows:

Operation	Definition
Depot	That level of logistics which has the facilities, personnel and capabilities to equal the quality of the equipment repair available at the contractor's facilities. (D)
Reference	That level in the maintenance of calibration equipment which provides DS and GS logistical support. (H)
Transfer	That level in the maintenance of calibration equipment which provides organizational and limited DS logistical support to Secondary Transfer equipment. (F)

MAINTENANCE ALLOCATION CHART

MAC PAGE

GROUP NUMBER	FUNCTIONAL GROUP	MAINTENANCE FUNCTIONS												
		a	b	c	d	e	f	g	h	i	j	k	l	m
		INSPECT	TEST	SERVICE	ADJUST	ALIGN	CALIBRATE	INSTALL	REPLACE	REPAIR	OVERHAUL	REBUILD	TOOL REQD.	REMARKS
1	Plug-In Dual Trace Sampling 3S1	F	F	F	-	-	F	F	F	F	D	-	1	A
2	Switch, Wired-Dual Trace	F	-	-	-	-	-	-	F	F	D	-	2	B
3	Switch, Wired mVolts/Div	F	-	-	-	-	-	-	F	F	D	-	3	B
4	Switch, Wired-Internal Trigger	F	-	-	-	-	-	-	F	F	D	-	3	B
5	Assembly, Circuit Board Channel A	F	-	-	-	-	-	-	F	F	D	-	4	C
6	Assembly Circuit Board Channel B	F	-	-	-	-	-	-	F	F	D	-	5	D
7	Assembly Circuit Board Strobe	F	-	-	-	-	-	-	F	F	D	-	6	E

TOOLS REQUIRED PAGE

TOOL CODE	CATEGORY	NOMENCLATURE	TOOL NUMBER
1-b	F	Generator, Pulse MIS-10215	4931-111-6681
	F	Generator, Square Wave MIS-10284	6625-455-5855
	F	Oscilloscope 7910655-2	6625-935-1313
	F	Plug-In Unit, Electrical 7910656-1	6625-246-9709
	F	Ratiometer, Digital 7910588-3	4931-913-3069
	F	Voltage Standard DC 7911393	4931-913-3062
	F	Adapter, Connector 7913001	5935-420-3645
	F	Adapter, Connector 10528559	4931-913-3214
	F	Adapter, Radio Frequency 7909471	5935-864-9988
	F	Cable Assembly, Radio Frequency 7907471	4931-739-4412
	F	Extension, Flexible 7911755	4931-916-5922
1-c	F	Cleaner, Electrical Contact	6850-973-3122
	F	Brush, Artist	8020-224-8022
	F	Brush, Dusting	7920-205-3571
	F	Cloth	7920-205-3571
1-f	F	Tool Kit	5180-650-7821
	F	Generator, Pulse MIS-10215	4931-111-6681
	F	Generator, Square Wave MIS-10284	6625-455-5855
	F	Oscilloscope 7910655-2	6625-935-1313
	F	Plug-In Unit, Electrical 7910656-1	6625-246-9709
	F	Ratiometer, Digital 7910588-3	4931-913-3069
	F	Voltage Standard, DC 7911393	4931-913-3062
	F	Adapter, Connector 7913001	5935-420-3645
	F	Adapter, Connector 10528559	4931-913-3214
	F	Adapter, Radio Frequency 7909411	4935-864-9988
	F	Cable Assembly, Radio Frequency 7907471	4931-739-4412
	F	Extension, Flexible 7911755	4931-916-5922
1-i	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
	F	Multimeter 7904729	6625-649-3290
	F	Impedance Measuring 7912149-2	4931-913-2897
	F	Cable Assembly, GR874 to GR874	4931-914-5949
	F	Semiconductor Tester with Probe	4931-914-5185
	F	Heat Sink	(28493) 30A
	F	Galvanometer 7910439	6625-510-1814

TOOLS REQUIRED PAGE - Continued

TOOL CODE	CATEGORY	NOMENCLATURE	TOOL NUMBER
	F	Power Supply, DC MIS-10230	4931-115-0567
	F	Cable Assembly, Radio Frequency 3 Required 7907470	4931-846-0010
1-j	D	Tool Kit	5180-650-7821
	D	Solder	3439-821-7674
	D	Multimeter 7904729	6625-649-3290
	D	Capacitance Measuring Assembly 7910842	4931-916-5952
	D	Cable Assembly, GR874 to GR874	4931-914-5949
	D	Semiconductor Tester with Probe	4931-914-5185
	D	Heat Sink	(28493) 30A
	D	Bridge, Resistance 7909149	4931-869-7997
	D	Detector, Galvanometer 7907452	4931-788-0021
	D	Power Supply, Precision 7907279	4931-778-3688
	D	Cable Assembly, Radio Frequency 3 Required 7907470	4931-846-0010
2-h	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
2-i	F	Multimeter 7904729	6625-649-3290
	F	Power Supply, DC MIS-10230	4931-115-0567
	F	Galvanometer 7910439	6625-510-1814
	F	Cable Assy, RF, 3 Required 7907470	4931-846-0010
	F	Tool Kit	5180-650-7821
	F	Impedance Measuring 7912149-2	4931-913-2993
	F	Solder	3439-821-7674
2-j	D	Multimeter 7904729	6625-649-3290
	D	Bridge, Resistance 7909149	4931-869-7997
	D	Power Supply, Precision 7907279	4931-778-3688
	D	Detector, Galvanometer 7907452	4931-788-0021
	D	Cable Assy, RF, 3 Required 7907470	4931-846-0010
	D	Tool Kit	5180-650-7821
	D	Solder	3439-821-7674
3-h	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
3-i	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
	F	Multimeter 7904729	6625-649-3290
	F	Impedance Measuring 7912149-2	4931-913-2897

TOOLS REQUIRED PAGE - Continued

TOOL CODE	CATEGORY	NOMENCLATURE	TOOL NUMBER
	F	Cable Assembly, GR874 to GR874	4931-914-5949
	F	Semiconductor Tester with Probe	4931-914-5185
	F	Heat Sink	(28493) 30A
	F	Galvanometer 7910439	6625-510-1814
	F	Power Supply, DC MIS-10230	4931-115-0567
	F	Cable Assembly, Radio Frequency 3 Required 7917470	4931-846-0010
3-j	D	Tool Kit	5180-650-7821
	D	Solder	3439-821-7674
	D	Multimeter 7904729	6625-649-3290
	D	Capacitance Measuring Assembly 7910842	4931-916-5952
	D	Cable Assembly, GR874 to GR874	4931-914-5949
	D	Semiconductor Tester with Probe	4931-914-5185
	D	Heat Sink	(28493) 30A
	D	Bridge, Resistance 7909149	4931-869-7997
	D	Detector, Galvanometer 7907452	4931-788-0021
	D	Power Supply, Precision 7907279	4931-778-3688
	D	Cable Assembly, Radio Frequency 3 Required 7907470	4931-846-0010
4-h	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
4-i	F	Power Supply, DC MIS-10230	4931-115-0567
	F	Galvanometer 7910439	6625-510-1814
	F	Cable Assembly, RF, 3 Required 7907470	4931-846-0010
	F	Multimeter 7904729	6625-649-3290
	F	Impedance Measuring 7912149-2	4931-913-2897
	F	Cable Assembly, GR874 to GR874	4931-914-5949
	F	Semiconductor Tester with Probe	4931-914-5185
	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
	F	Heat Sink	(28493) 30A
4-j	D	Resistance 7909149	4931-869-7997
	D	Power Supply, Precision 7907279	4931-778-3688
	D	Detector, Galvanometer 7907452	4931-788-0021
	D	Cable Assembly, RF, 3 Required 7907470	4931-846-0010
	D	Multimeter 7904729	6625-649-3290
	D	Capacitance Measuring Assembly 7910842	4931-916-5952

TOOLS REQUIRED PAGE - Continued

TOOL CODE	CATEGORY	NOMENCLATURE	TOOL NUMBER
	D	Cable Assembly, GR874 to GR874	4931-914-5949
	D	Semiconductor Tester with Probe	4931-914-5185
	D	Bridge, Inductance 7907184-1	6625-777-4118
	D	Tool Kit	5180-650-7821
	D	Solder	3439-821-7674
	D	Heat Sink	(28493) 30A
5-h	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
5-i	F	Power Supply, DC MIS-10230	4931-115-0567
	F	Galvanometer 7910439	6625-510-1814
	F	Cable Assembly, RF, 3 Required 7907470	4931-846-0010
	F	Multimeter 7904729	6625-649-3290
	F	Impedance Measuring 7912149-2	4931-913-2897
	F	Cable Assembly, GR874 to GR874	4931-914-5949
	F	Semiconductor Tester with Probe	4931-914-5185
	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
	F	Heat Sink	(28493) 30A
5-j	D	Bridge, Resistance 7909149	4931-869-7997
	D	Power Supply, Precision 7907279	4931-778-3688
	D	Detector, Galvanometer	4931-788-0021
	D	Cable Assembly, RF, 3 Required 7907470	4931-846-0010
	D	Multimeter 7904729	6625-649-3290
	D	Capacitance Measuring Assembly 7910842	4931-916-5952
	D	Cable Assembly, GR874 to GR874	4931-914-5949
	D	Semiconductor Tester with Probe	4931-914-5185
	D	Bridge, Inductance 7907184-1	6625-777-4118
	D	Tool Kit	5180-650-7821
	D	Solder	3439-821-7674
	D	Heat Sink	(28493) 30A
6-h	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
6-i	F	Power Supply, DC MIS-10230	4931-115-0567
	F	Galvanometer 7910439	6625-510-1814
	F	Cable Assembly, RF, 3 Required 7907470	4931-846-0010

TOOLS REQUIRED PAGE - Continued

TOOL CODE	CATEGORY	NOMENCLATURE	TOOL NUMBER
	F	Multimeter 7904729	6625-649-3290
	F	Impedance Measuring 7912149-2	4931-913-2897
	F	Cable Assembly, GR874 to GR874	4931-914-5949
	F	Semiconductor Tester with Probe	4931-914-5185
	F	Tool Kit	5180-650-7821
	F	Solder	3439-821-7674
	F	Heat Sink	(28493) 30A
6-j	D	Bridge, Resistance 7909149	4931-869-7997
	D	Power Supply, Precision 7907279	4931-778-3688
	D	Detector, Galvanometer 7907452	4931-788-0021
	D	Cable Assembly, RF, 3 Required 7907470	4931-846-0010
	D	Multimeter 7904729	6625-649-3290
	D	Capacitance Measuring Assembly 7910842	4931-916-5952
	D	Cable Assembly, GR874 to GR874	4931-914-5949
	D	Semiconductor Tester with Probe	4931-914-5185
	D	Bridge, Inductance 7907184-1	6625-777-4118
	D	Tool Kit	5180-650-7821
	D	Solder	3439-821-7674
	D	Heat Sink	(28493) 30A

REMARKS PAGE

REMARKS CODE	REMARKS
A-b	Test in accordance with Section 2 of TB 9-6625-965-50.
A-c	Clean components and case in accordance with Section 12 of TM 9-6625-965-14-1.
A-f	Calibrate in accordance with Section 3 of TB 9-6625-965-50.
A-g	Install in case No. 26 of Calibration Van (M292A5).
A-i	Solder all connections per MIL-S-45743.
A-j	Solder all connections per MIL-S-45743.
B-h	Solder all connections per MIL-S-45743.
B-i	Solder all connections per MIL-S-45743.
B-j	Solder all connections per MIL-S-45743.
C-h	Solder all connections per MIL-S-45743.
C-i	Solder all connections per MIL-S-45743.
C-j	Solder all connections per MIL-S-45743.
D-h	Solder all connections per MIL-S-45743.
D-i	Solder all connections per MIL-S-45743.
D-j	Solder all connections per MIL-S-45743.
E-h	Solder all connections per MIL-S-45743.
E-i	Solder all connections per MIL-S-45743.
E-j	Solder all connections per MIL-S-43743.

By Order of the Secretary of the Army:

BRUCE PALMER, JR.
General, United States Army
Acting Chief of Staff

Official:

VERNE L. BOWERS
Major General, United States Army
The Adjutant General

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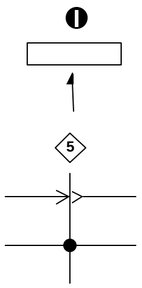
SECTION 11

DIAGRAMS

The following symbols are used on the diagrams:



Screwdriver adjustment

Front- or rear panel control or connector

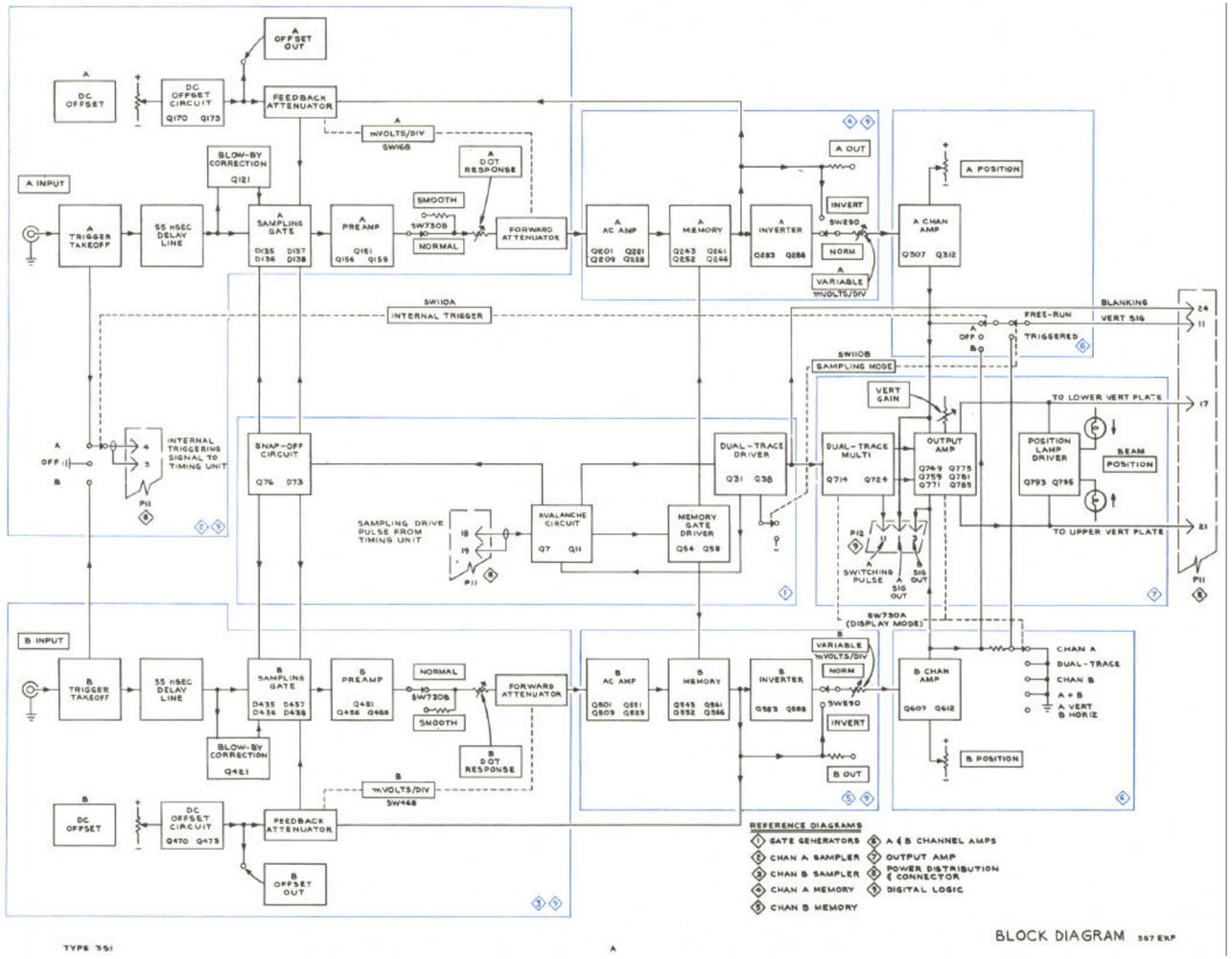
Clockwise control rotation in direction of arrow

Refer to indicated diagram

Connection to circuit board made with pin connector at indicated pin

Connection soldered to circuit board

Blue line encloses components located on circuit board



VOLTAGE AND WAVEFORM TEST CONDITIONS

Typical voltage measurements and waveform photographs (shown in blue) were obtained under the following conditions unless noted otherwise on the individual diagrams:

Test Oscilloscope

Bandwidth	DC to 33 MHz
Probe Input Impedance	10 Megohms, 7 picofarads
Probe Ground Lead	Clipped to Type 3S1 chassis
Triggering	Internal unless indicated otherwise

DC Voltmeter

Type	Volt-Ohmmeter
Sensitivity	20,000 Ω/volt

Type 3S1 Conditions

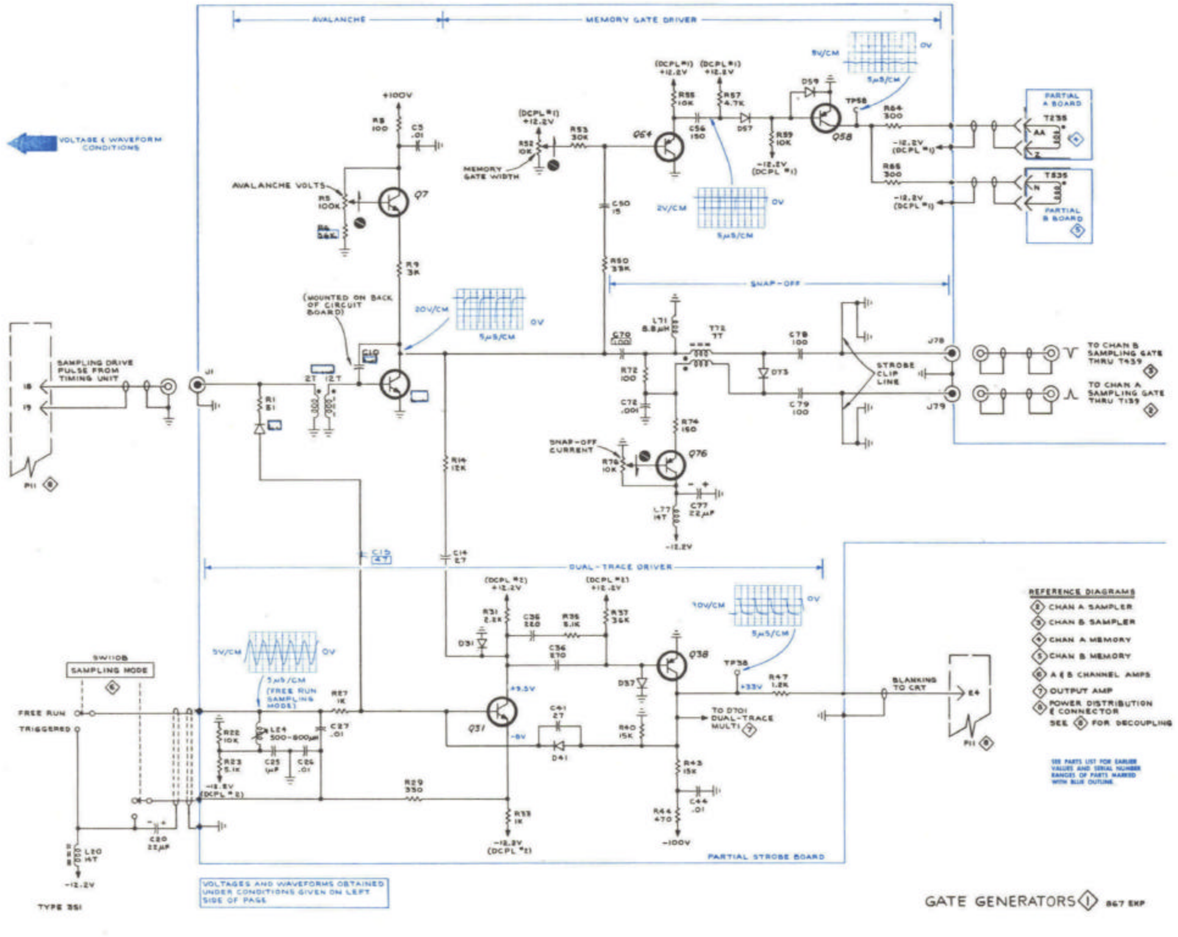
	Connected to oscilloscope through 30-inch flexible extension (Tektronix Part No. 012-0066-00)
Vertical Input Signal	None
External Triggering Signal	None

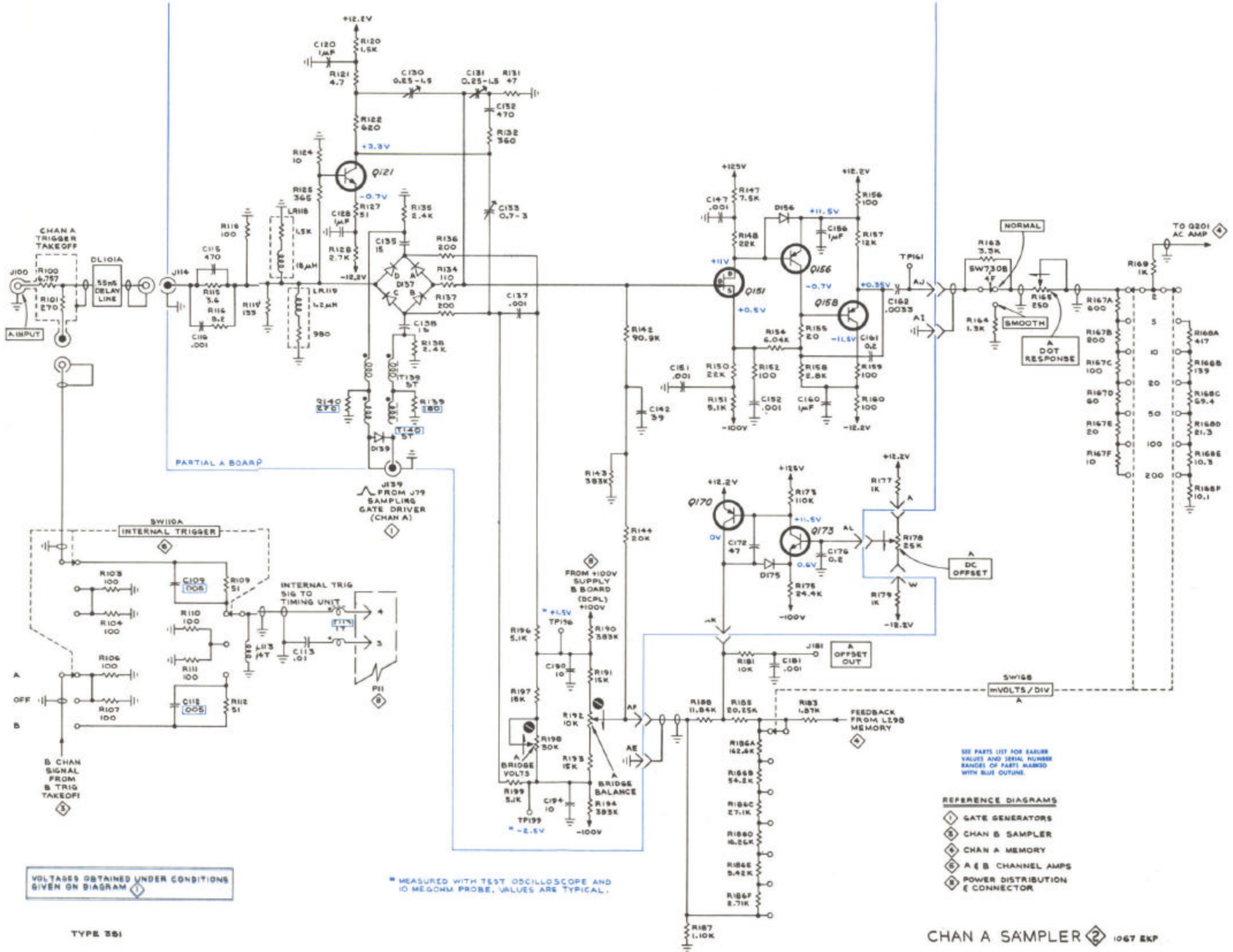
Type 3S1 Control Settings

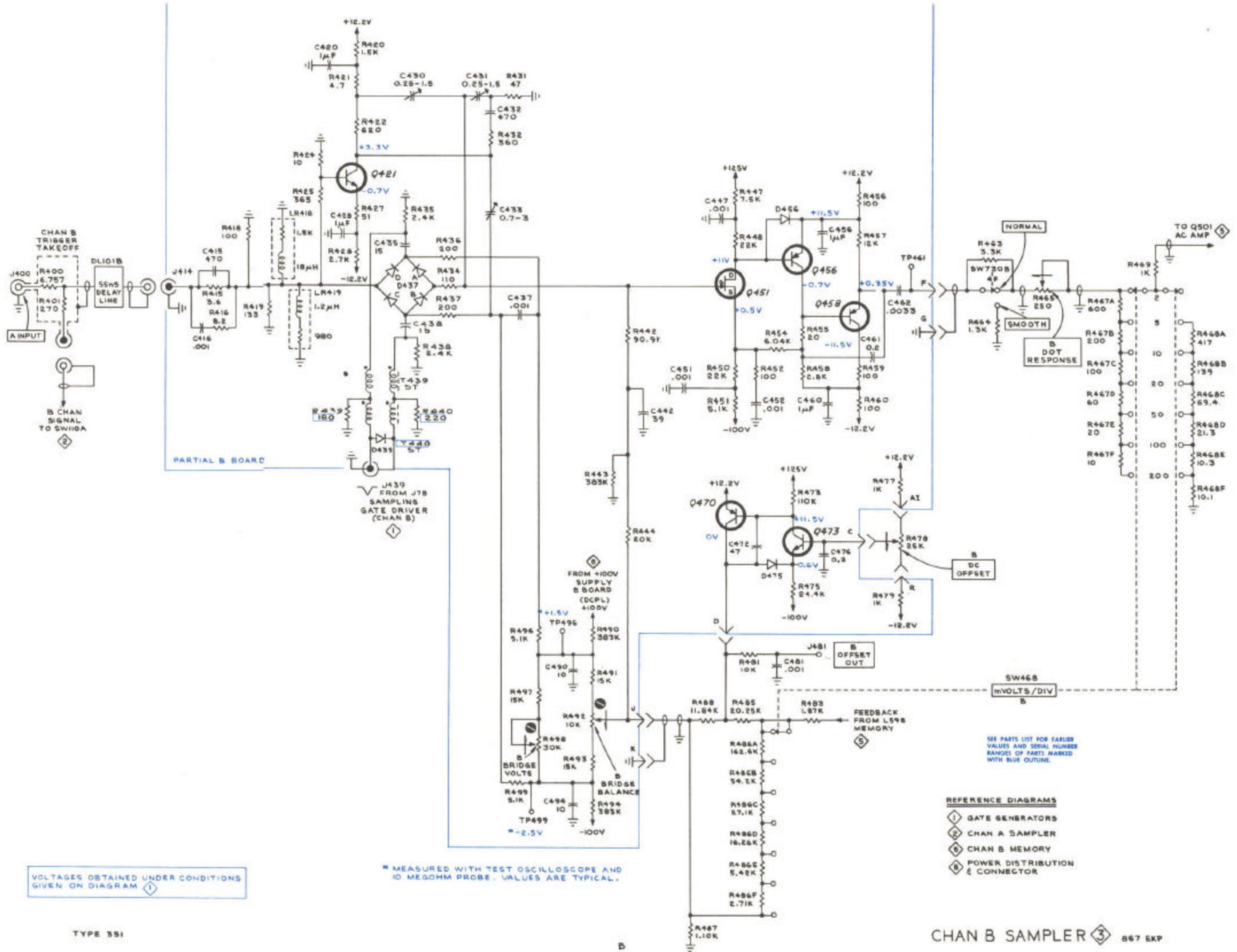
mVolts/DIV	200
mVolts/Div VARIABLE	CAL (at detent)
Vertical POSITION	Centered
DC OFFSET ±1 V	Zero volts at OFFSET OUT
SMOOTH-NORMAL	NORMAL
INVERT-NORM	NORM
SAMPLING MODE	TRIGGERED
DISPLAY MODE	CHAN A (CHAN B)
INTERNAL TRIGGER	A

Type 3T77A Sampling Sweep plug-in

Trigger Sensivity	Clockwise
Dots/div	100
Trigger Mode	Int
TIME/DIV	50 nSEC




CHAN A TRIGGER TAKEOFF
J100
A INPUT
R100 6.75?
R101 270
DL101A 55nS DELAY LINE
J114
C115 470
R115 5.6
R116 8.2
C116 .001
R116 100
R117 133
LR118 1.5K 18µH
LR119 42µH 980
+12.2V
C120 1µF
R120 1.5K
R121 4.7
C130 0.25-1.5
C131 0.25-1.5
R131 47
C132 470
R132 360
R122 620
+3.3V
Q121
R124 10
R125 365
C128 1µF
R127 51
R128 2.7K
-12.2V
-0.7V
R135 2.4K
C133 0.7-3
C135 15
R136 200
R134 110
D137
R137 200
C137 .001
C138 15
R138 2.4K
T139 5T
R139 180
R140 270
T140 5T
D139
J139 FROM J79 SAMPLING GATE DRIVER (CHAN A)
PARTIAL A BOARD
SW110A INTERNAL TRIGGER
R103 100
R104 100
C109 .005
R109 51
R110 100
R111 100
C113 .01
L113 4T
INTERNAL TRIG SIG TO TIMING UNIT
T114 1T
P11
R106 100
R107 100
C112 .005
R112 51
A
OFF
B
B CHAN SIGNAL FROM B TRIG TAKEOFF
R142 90.9K
C142 39
R143 383K
R144 20K
+125V
R147 7.5K
C147 .001
R148 22K
D156
+11.5V
C156 1µF
Q156
R156 100
R157 12K
+11V
Q151
+0.5V
-0.7V
Q158
+0.35V
TP161
C162 .0033
A1
R154 6.04K
R155 20
-11.5V
C161 0.2
C151 .001
R150 22K
R151 5.1K
-100V
R152 100
C152 .001
R158 2.8K
C160 1µF
R159 100
R160 100
-12.2V
+12.2V
Q170
0V
+125V
R173 110K
+11.5V
Q173
R177 1K
A
R178 25K
AL
DC OFFSET
W
R179 1K
-12.2V
C172 47
D175
0.6V
R175 24.9K
-100V
FROM +100V SUPPLY B BOARD (DCPL) +100V
+1.5V
TP196
R196 5.1K
R190 383K
C190 10
R191 15K
R197 15K
R192 10K
AF
AE
R198 50K
A BRIDGE VOLTS
R193 15K
BRIDGE BALANCE
R199 5.1K
C194 10
R194 383K
TP199
-2.5V
-100V
J181
A OFFSET OUT
R181 10K
C181 .001
R188 11.84K
R185 20.25K
R183 1.87K
FEEDBACK FROM LZ98 MEMORY
SW168 mVOLTS/DIV
A
R186A 162.6K
R186B 54.2K
R186C 27.1K
R186D 16.25K
R186E 5.42K
R186F 2.71K
R187 1.10K
NORMAL
R163 3.3K
SW7308 4F
R165 250
SMOOTH
R164 1.3K
A DOT RESPONSE
TO Q201 AC AMP
R169 1K
R167A 400
R167B 200
R167C 100
R167D 80
R167E 20
R167F 10
5
10
20
50
100
200
R168A 417
R168B 139
R168C 69.4
R168D 21.3
R168E 10.3
R168F 10.1
VOLTAGES OBTAINED UNDER CONDITIONS GIVEN ON DIAGRAM 1
* MEASURED WITH TEST OSCILLOSCOPE AND 10 MEGOHM PROBE. VALUES ARE TYPICAL.
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
REFERENCE DIAGRAMS
1 GATE GENERATORS
3 CHAN B SAMPLER
4 CHAN A MEMORY
6 A & B CHANNEL AMPS
8 POWER DISTRIBUTION & CONNECTOR
TYPE 351
CHAN A SAMPLER 2 1067 EKP



VOLTAGES OBTAINED UNDER CONDITIONS GIVEN ON DIAGRAM (1)

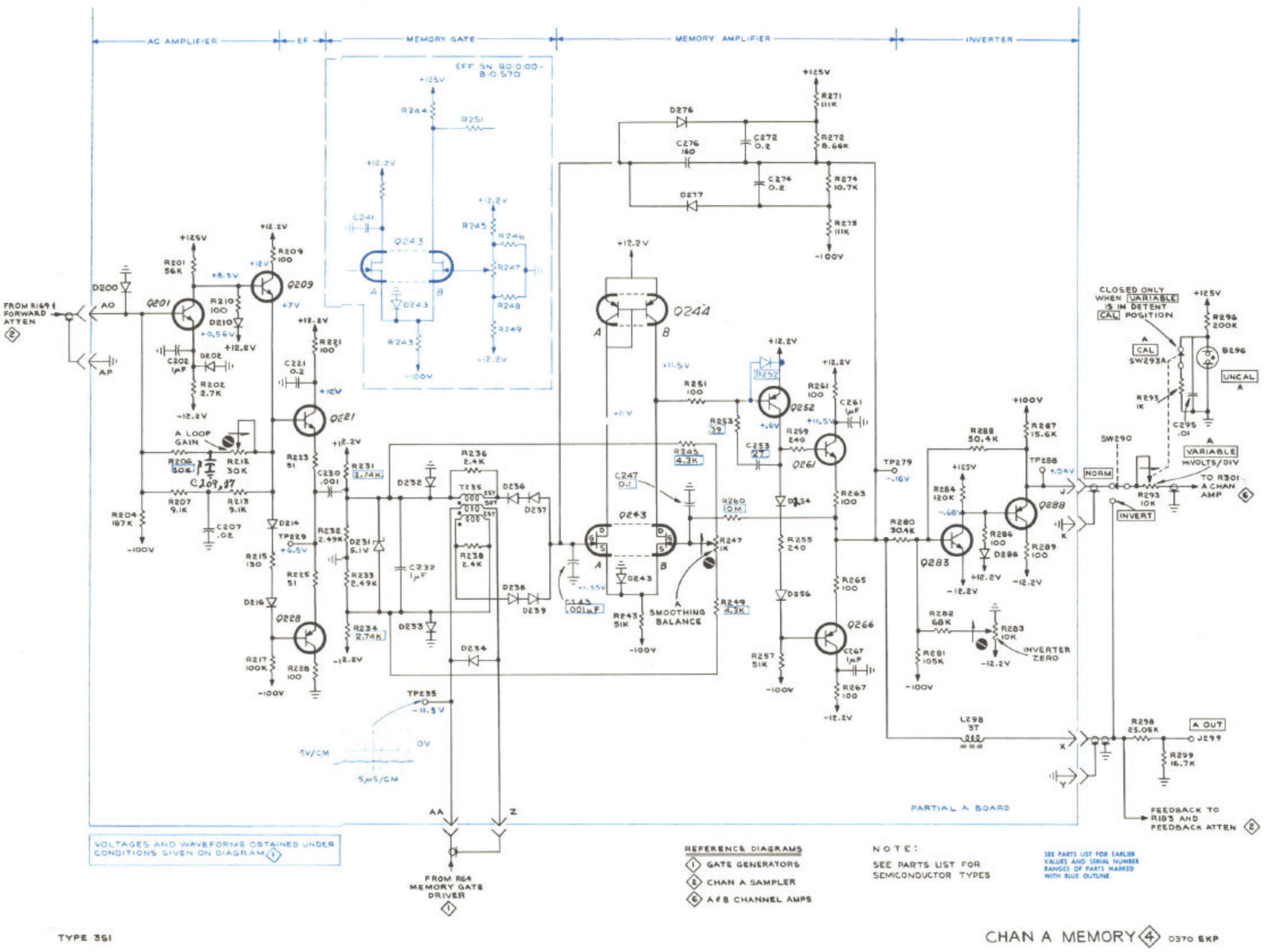
* MEASURED WITH TEST OSCILLOSCOPE AND 10 MEGOHM PROBE. VALUES ARE TYPICAL.

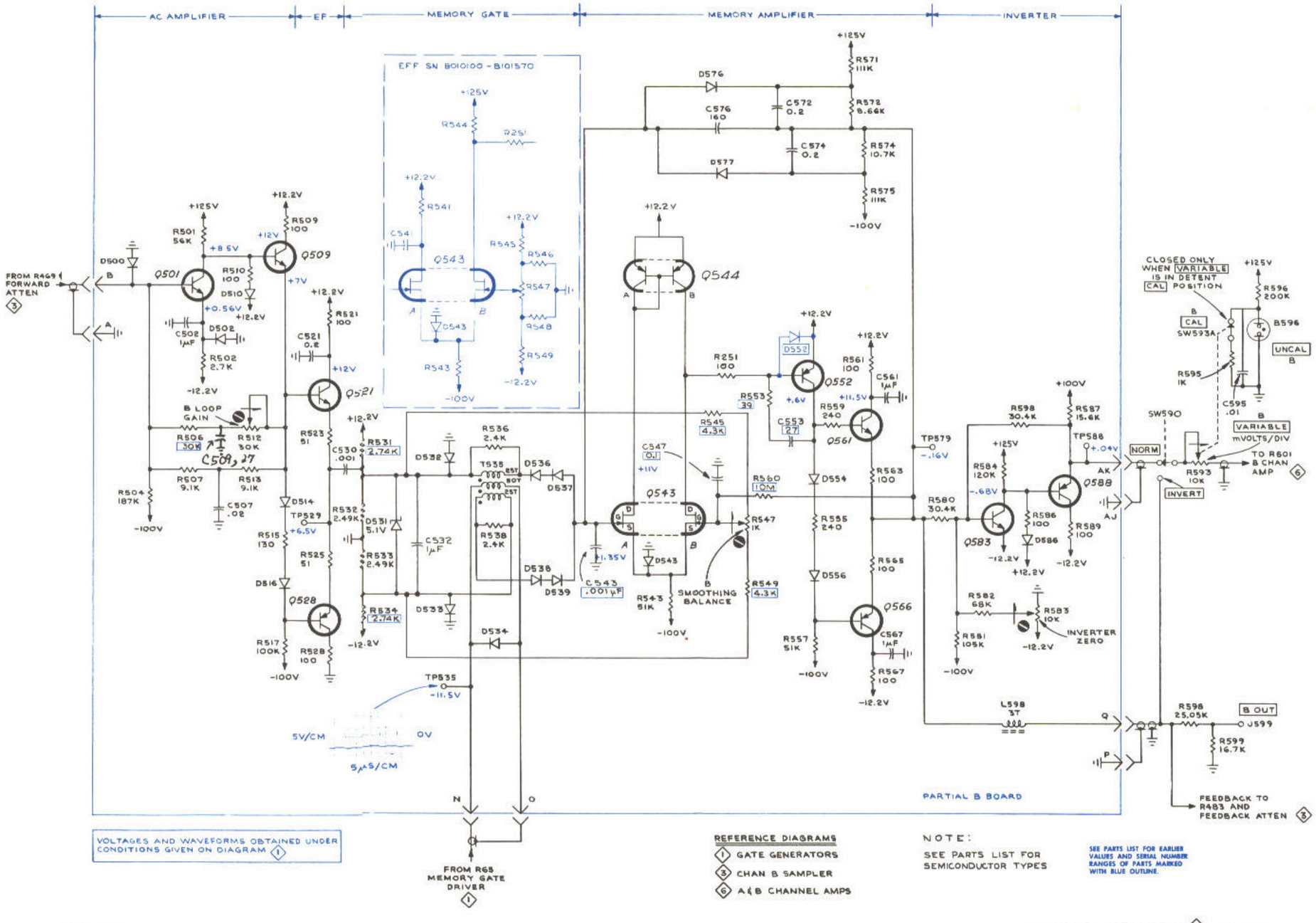
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

REFERENCE DIAGRAMS
(1) GATE GENERATORS
(2) CHAN A SAMPLER
(3) CHAN B MEMORY
(4) POWER DISTRIBUTION & CONNECTOR

CHAN B SAMPLER (3) 867 EKP

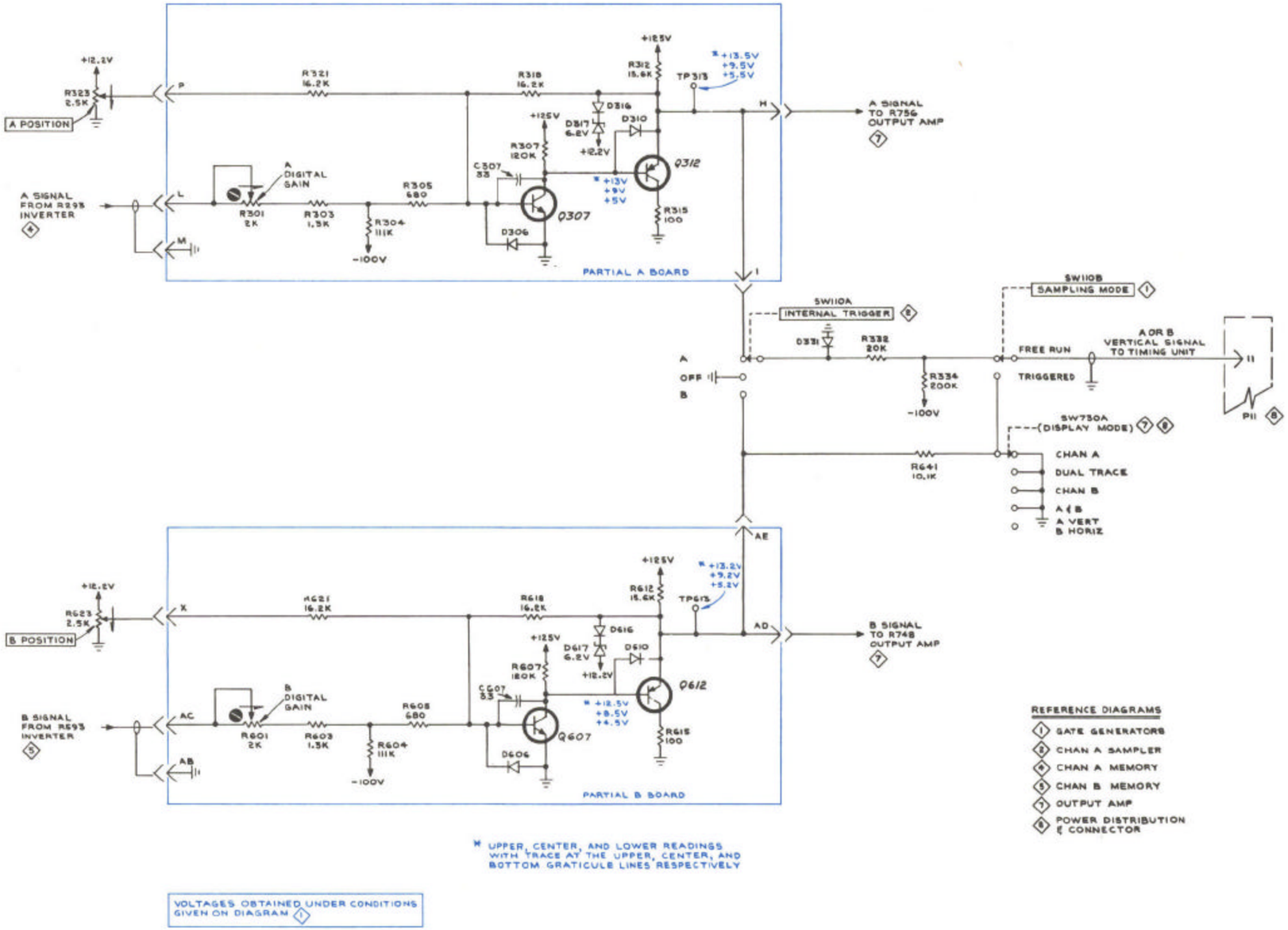
TYPE 551

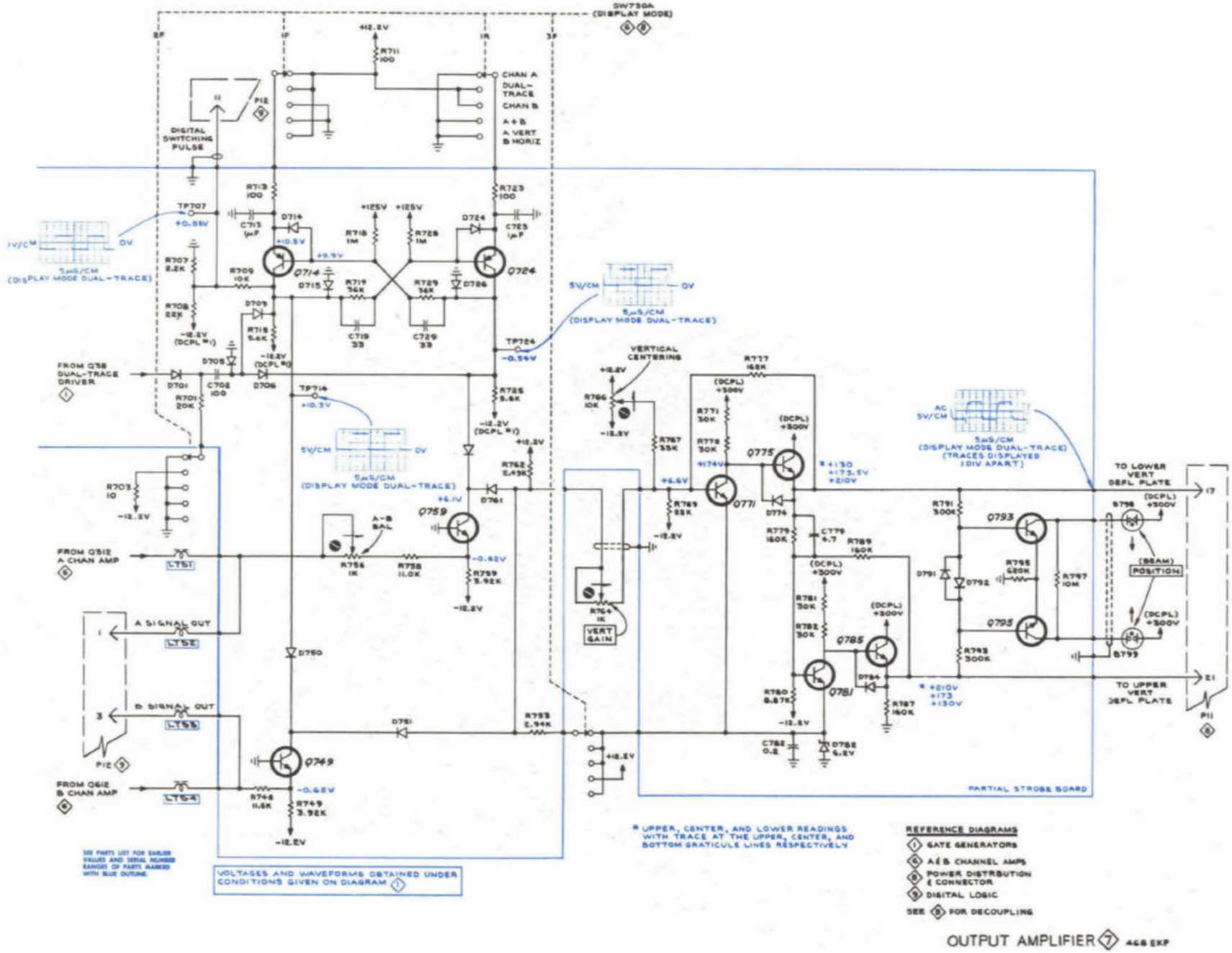

AC AMPLIFIER
EF
MEMORY GATE
MEMORY AMPLIFIER
INVERTER
EFF SN B010100-B010370
FROM R169 FORWARD ATTEN
A LOOP GAIN
SMOOTHING BALANCE
INVERTER ZERO
CLOSED ONLY WHEN VARIABLE IS IN DETENT CAL POSITION
NORM
INVERT
VARIABLE mVOLTS/DIV
TO R301 A CHAN AMP
FEEDBACK TO R183 AND FEEDBACK ATTEN
FROM R64 MEMORY GATE DRIVER
PARTIAL A BOARD
VOLTAGES AND WAVEFORMS OBTAINED UNDER CONDITIONS GIVEN ON DIAGRAM 1
REFERENCE DIAGRAMS
1 GATE GENERATORS
2 CHAN A SAMPLER
6 A & B CHANNEL AMPS
NOTE:
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
TYPE 351
CHAN A MEMORY 4 0370 EKP

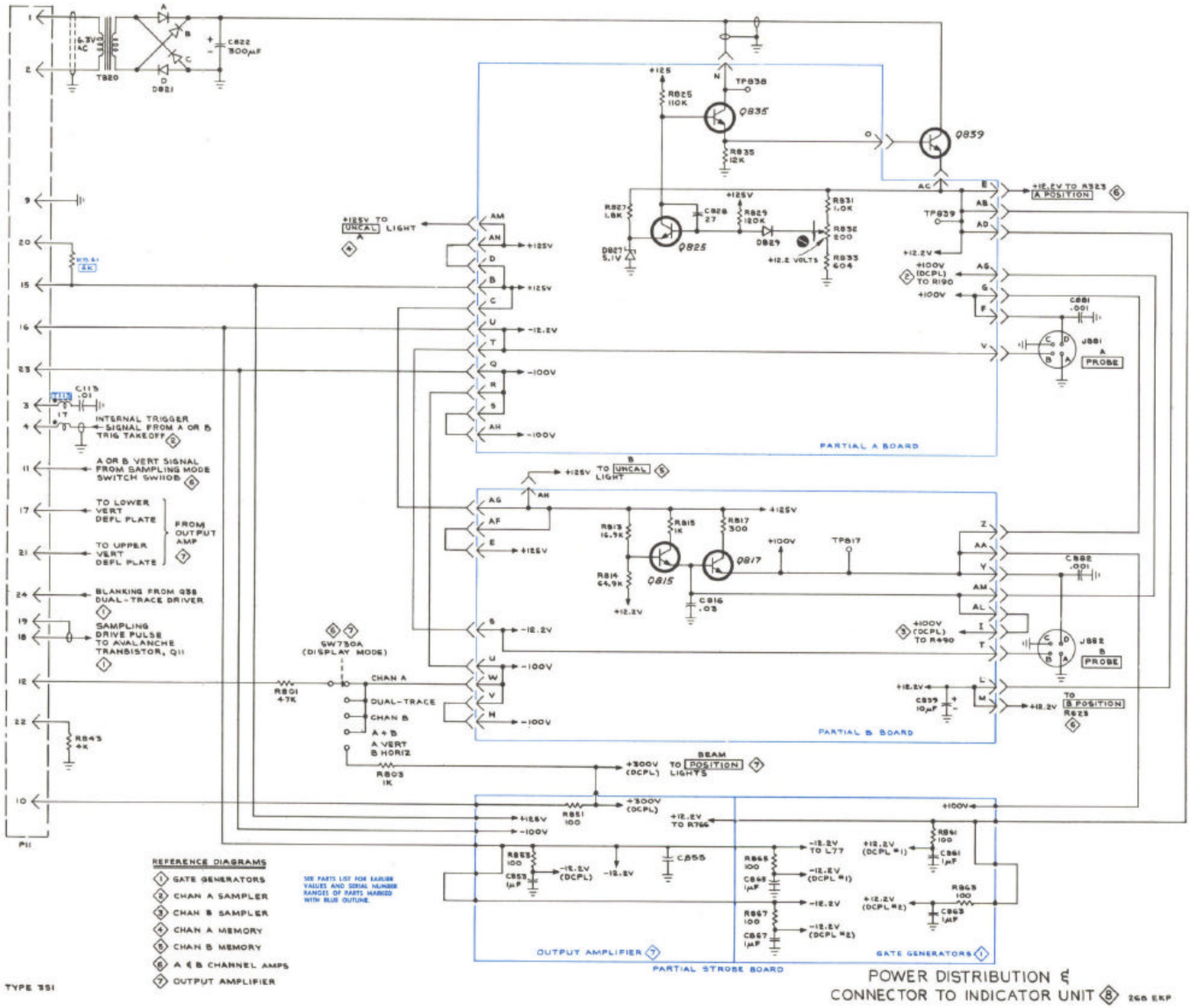


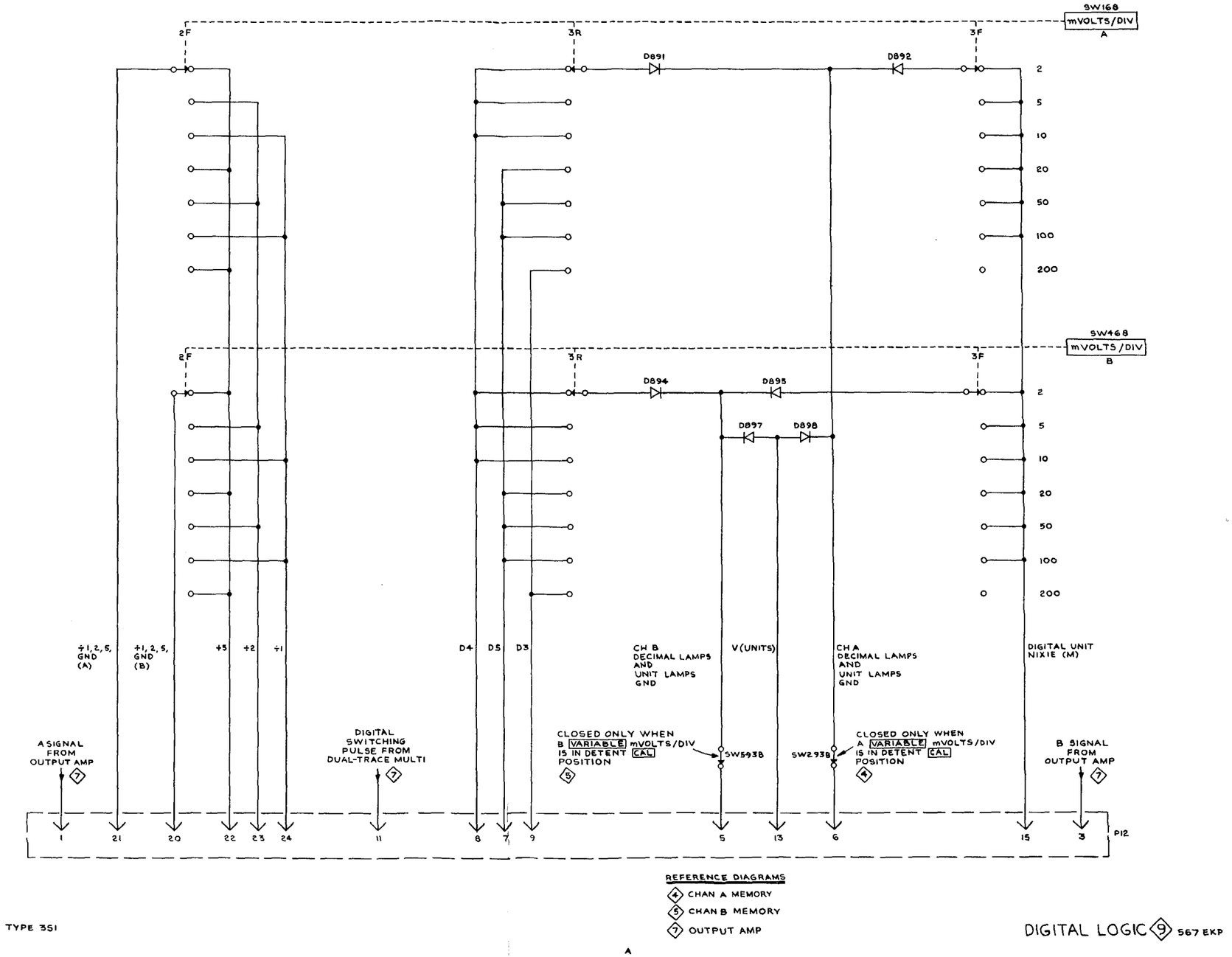
TYPE 391

CHAN B MEMORY 5 0370 EKP


+12.2V
R323 2.5K
A POSITION
P
R321 16.2K
R318 16.2K
+125V
R312 15.6K
TP313
*+13.5V +9.5V +5.5V
D316
D317 6.2V
D310
+12.2V
H
A SIGNAL TO R756 OUTPUT AMP
7
R307 120K
C307 33
+125V
*+13V +9V +5V
Q312
A DIGITAL GAIN
A SIGNAL FROM R293 INVERTER
4
L
M
R301 2K
R303 1.3K
R305 680
R304 111K
-100V
Q307
D306
R315 100
PARTIAL A BOARD
I
SW110A
INTERNAL TRIGGER
8
SW110B
SAMPLING MODE
1
D331
R332 20K
A
OFF
B
FREE RUN
TRIGGERED
A OR B VERTICAL SIGNAL TO TIMING UNIT
11
P11
8
R334 200K
-100V
SW730A
(DISPLAY MODE)
7
8
R641 10.1K
CHAN A
DUAL TRACE
CHAN B
A & B
A VERT
B HORIZ
AE
+12.2V
X
R621 16.2K
R618 16.2K
+125V
R612 15.6K
*+13.2V +9.2V +5.2V
TP613
D616
D617 6.2V
D610
+12.2V
AD
B SIGNAL TO R748 OUTPUT AMP
7
R607 120K
C607 33
+125V
*+12.5V +8.5V +4.5V
Q612
B SIGNAL FROM R593 INVERTER
5
AC
AB
B DIGITAL GAIN
R601 2K
R603 1.3K
R605 680
R604 111K
-100V
Q607
D606
R615 100
PARTIAL B BOARD
REFERENCE DIAGRAMS
1 GATE GENERATORS
2 CHAN A SAMPLER
4 CHAN A MEMORY
5 CHAN B MEMORY
7 OUTPUT AMP
8 POWER DISTRIBUTION & CONNECTOR
* UPPER, CENTER, AND LOWER READINGS WITH TRACE AT THE UPPER, CENTER, AND BOTTOM GRATICULE LINES RESPECTIVELY
VOLTAGES OBTAINED UNDER CONDITIONS GIVEN ON DIAGRAM 1


SW730A (DISPLAY MODE)
2F
1F
1R
3F
+12.2V
R711 100
CHAN A DUAL-TRACE
CHAN B
A + B
A VERT B HORIZ
P12
DIGITAL SWITCHING PULSE
R713 100
R723 100
TP707
+0.05V
C713 1μF
C723 1μF
D714
D724
+12.5V
+12.5V
R718 1M
R728 1M
Q714
Q724
+9.9V
R707 2.2K
R709 10K
R719 36K
R729 36K
D715
D726
C719 33
C729 33
R708 22K
D709
R715 5.6K
-12.2V (DCPL #1)
-12.2V (DCPL #2)
TP724
-0.54V
FROM Q58 DUAL-TRACE DRIVER
D701
D705
D706
C702 100
R701 20K
TP714
+10.3V
R725 5.6K
R703 10
-12.2V
5V/CM
0V
5μS/CM (DISPLAY MODE DUAL-TRACE)
+12.2V
R762 2.43K
D761
+6.1V
Q759
A-B BAL
R756 1K
R758 11.0K
R759 3.92K
-0.62V
-12.2V
FROM Q512 A CHAN AMP
LT51
A SIGNAL OUT
LT52
B SIGNAL OUT
LT53
LT54
FROM Q612 B CHAN AMP
D750
D751
R753 2.94K
Q749
R748 11.8K
R749 3.92K
-0.62V
-12.2V
+12.2V
VERTICAL CENTERING
R766 10K
R767 33K
R777 162K
(DCPL) +300V
R771 30K
R778 30K
+6.6V
+174V
Q775
Q771
D774
R769 88K
R779 160K
C779 4.7
R789 160K
R781 30K
R782 30K
Q785
Q781
D784
R780 8.87K
R787 160K
C782 0.2
D788 6.8V
* +130 +173.5V +210V
* +210V +173 +130V
VERT GAIN
R764 1K
AC 5V/CM
5mS/CM (DISPLAY MODE DUAL-TRACE) (TRACES DISPLAYED 1 DIV APART)
TO LOWER VERT DEFL PLATE
TO UPPER VERT DEFL PLATE
Q793
Q795
D791
D792
R791 300K
R795 620K
R797 10M
R793 300K
B798
B799
(BEAM) POSITION
P11
PARTIAL STROBE BOARD
* UPPER, CENTER, AND LOWER READINGS WITH TRACE AT THE UPPER, CENTER, AND BOTTOM GRATICULE LINES RESPECTIVELY
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE
VOLTAGES AND WAVEFORMS OBTAINED UNDER CONDITIONS GIVEN ON DIAGRAM 1
REFERENCE DIAGRAMS
1 GATE GENERATORS
6 A & B CHANNEL AMPS
8 POWER DISTRIBUTION & CONNECTOR
9 DIGITAL LOGIC
SEE 8 FOR DECOUPLING
OUTPUT AMPLIFIER 7 468 EXP


T820
D821
C822 800μF
+125
TP838
R825 110K
Q835
R835 12K
Q839
+12.2V TO R323 A POSITION
R827 1.8K
C828 .27
R829 120K
D829
R831 1.0K
R832 200
R833 604
Q825
D827 5.1V
+12.2 VOLTS
TP839
+12.2V
+100V (DCPL) TO R190
+100V
C881 .001
J881 A PROBE
+125V TO UNCAL LIGHT
PARTIAL A BOARD
INTERNAL TRIGGER SIGNAL FROM A OR B TRIG TAKEOFF
A OR B VERT SIGNAL FROM SAMPLING MODE SWITCH SW110B
TO LOWER VERT DEFL PLATE
TO UPPER VERT DEFL PLATE
FROM OUTPUT AMP
BLANKING FROM Q38 DUAL-TRACE DRIVER
SAMPLING DRIVE PULSE TO AVALANCHE TRANSISTOR, Q11
R843 4K
P11
SW730A (DISPLAY MODE)
R801 4.7K
CHAN A
DUAL-TRACE
CHAN B
A+B
A VERT B HORIZ
R803 1K
+125V TO UNCAL LIGHT
R813 16.9K
R815 1K
R817 300
Q815
Q817
R814 64.9K
C816 .03
TP817
+100V
C888 .001
J882 B PROBE
+100V (DCPL) TO R490
C839 10μF
TO B POSITION R623
+300V (DCPL) TO BEAM POSITION LIGHTS
R851 100
+300V (DCPL)
+12.2V TO R766
R853 100
C853 1μF
-12.2V (DCPL)
C855
R865 100
C865 1μF
-12.2V TO L77
-12.2V (DCPL #1)
R867 100
C867 1μF
-12.2V (DCPL #2)
R861 100
C861 1μF
+12.2V (DCPL #1)
R863 100
C863 1μF
+12.2V (DCPL #2)
OUTPUT AMPLIFIER
GATE GENERATORS
PARTIAL B BOARD
PARTIAL STROBE BOARD
REFERENCE DIAGRAMS
1 GATE GENERATORS
2 CHAN A SAMPLER
3 CHAN B SAMPLER
4 CHAN A MEMORY
5 CHAN B MEMORY
6 A & B CHANNEL AMPS
7 OUTPUT AMPLIFIER
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
TYPE 351
POWER DISTRIBUTION & CONNECTOR TO INDICATOR UNIT 8 265 EKP

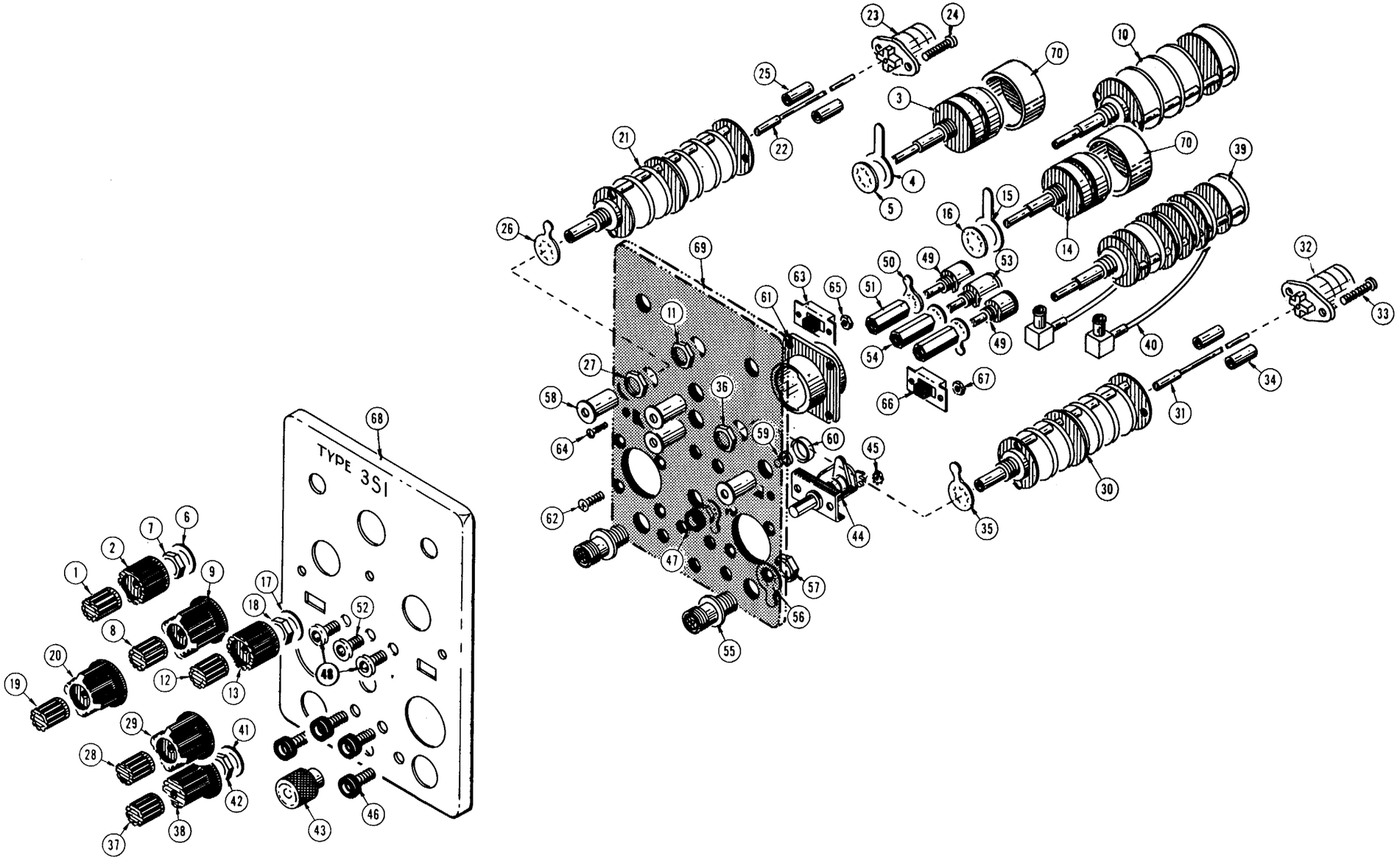


TYPE 351

DIGITAL LOGIC 9 567 EKP

A

FIG. 1. FRONT



B

FIG. 2. DELAY-LINE ASSEMBLY

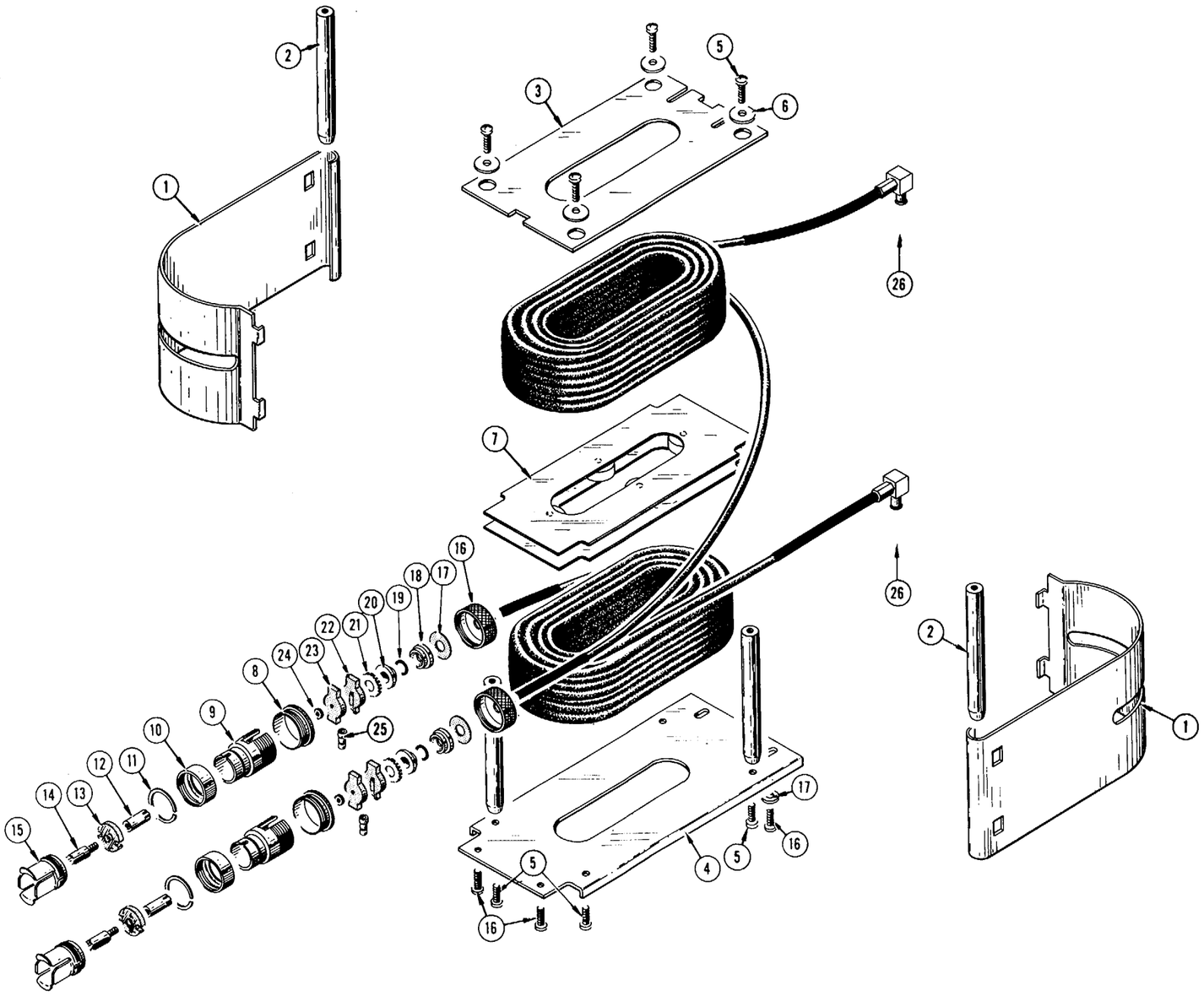


FIG. 3. CHASSIS & REAR

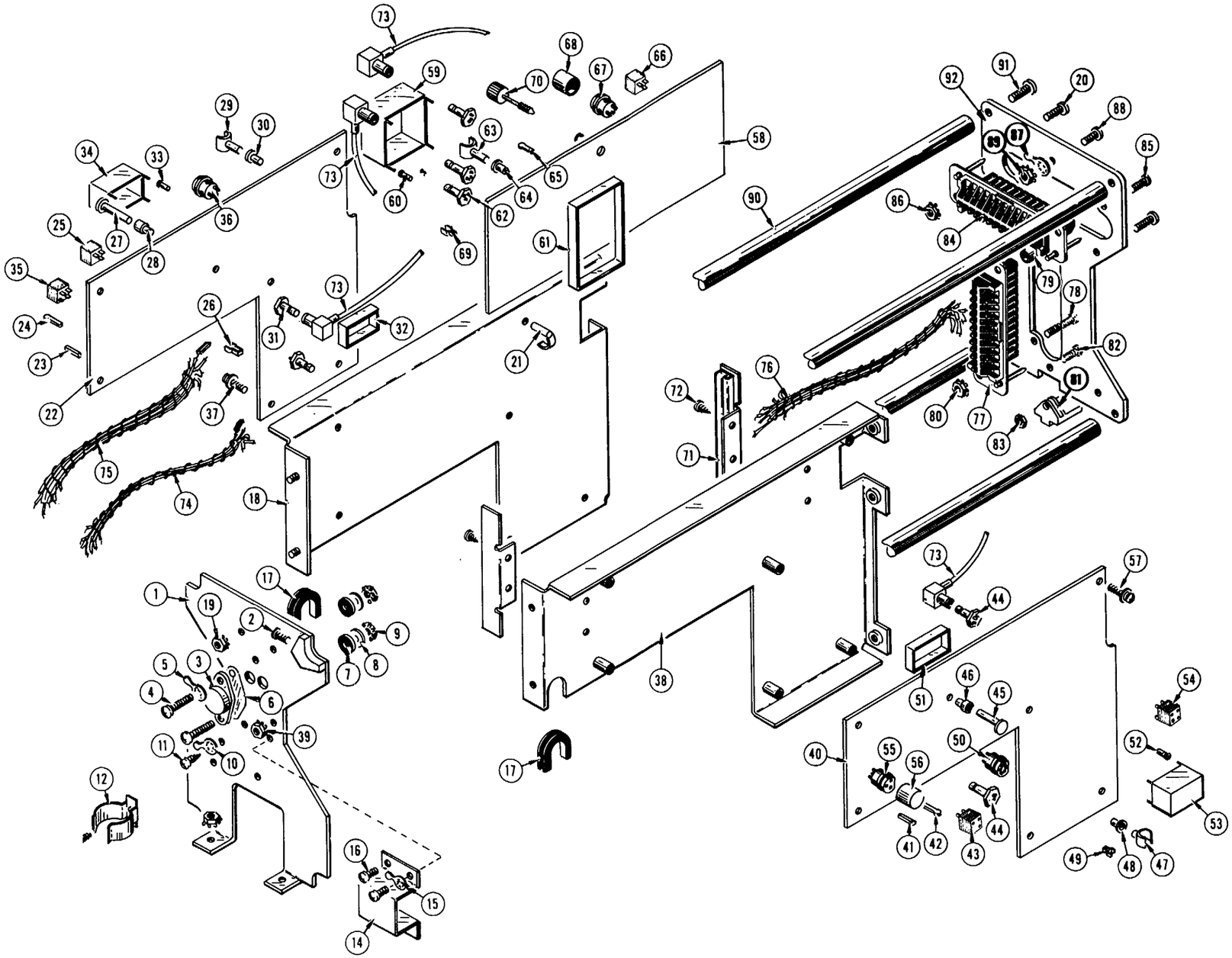
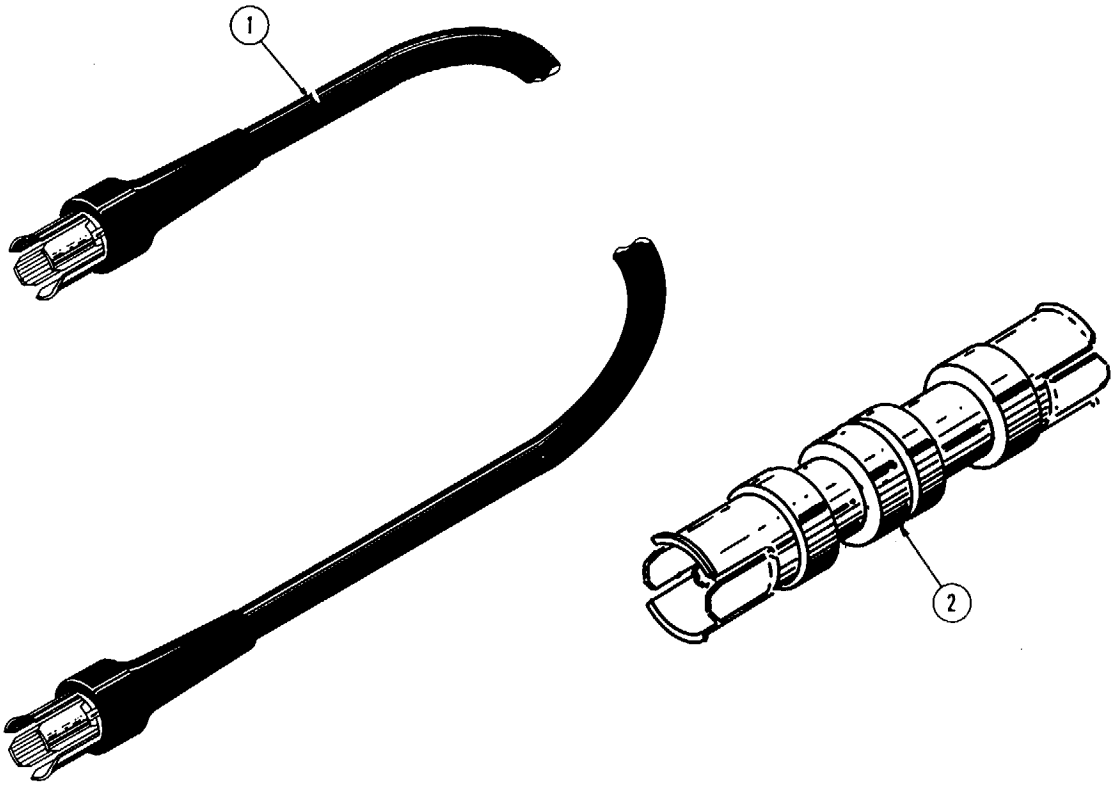


FIG. 4. STANDARD ACCESSORIES



B

Fig. & Index No.	Tektronix. Part No.	Serial/Model No. Eff	Disc	Qty	Description 1 2 3 4 5
4-1	017-0512-00	B010100	B049999	2	CABLE, 50 Ω, 5 Nsec
	017-0512-00	B050000		2	CABLE, 50 Ω,. 5 Nsec
-2	017-0078-00	XB05000		2	ATTENUATOR, 50 Ω, 10X, GR
	070-0632-00			2	MANUAL, instruction (not shown)